

AGN0944Q Data Sheet

X Band Power Amplifier MMIC

1. Product Overview

1.1 General Description

AGN0944Q is a two-stage internally matched MMIC Power Amplifier which operates between 8.5 GHz and 10 GHz frequency range. This product is well suited to X-band applications. AGN0944Q is packaged in a 6x6 mm air-cavity QFN. This product is well suited to Point to Point Radio and Communications.

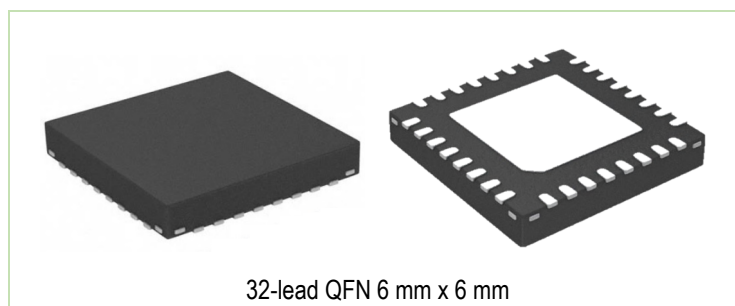
1.2 Features

- Frequency Range: 8.5 - 10 GHz
- Saturated Output Power: 43 dBm
- Power Added Efficiency: 32%
- Power Gain: 13 dB
- Small Signal Gain: 18 dB
- Bias: VDD = +24 V, IDD = 300 mA, VGG = -2.35 V (Typical)

1.3 Applications

- Point to Point Radio
- Communications

1.4 Package Profile



2. Summary on Product Performances

2.1 Typical Performance (Pulsed mode)

Test conditions : T = +25°C, VDD = +24 V, Pulse width = 100 μ s, Duty cycle = 10%.

Parameters	Test Conditions	Min	Typ	Max	Units
Gate Bias Voltage	$f = 8.5 - 10$ GHz		-2.35		V
Output Power at Psat ¹⁾	$f = 8.5 - 10$ GHz		43		dBm
Power Gain at Psat ¹⁾	$f = 8.5 - 10$ GHz		13		dB
Drain Current at Psat ¹⁾	$f = 8.5 - 10$ GHz		3200		mA
Power Added Efficiency at Psat ¹⁾	$f = 8.5 - 10$ GHz		32		%
Small Signal Gain	$f = 8.5 - 10$ GHz		18		dB
Input Return Loss	$f = 8.5 - 10$ GHz		-12		dB
Output Return Loss	$f = 8.5 - 10$ GHz		-12		dB
Drain Current			300		mA

1) Psat: Saturated output power

2.2 Absolute Maximum Ratings (not simultaneous) at 25°C

Parameters	Max. Ratings
Operating Case Temperature (Tc)	-40 to +85°C
Storage Temperature (Tstg)	-55 to +125°C
Drain Voltage (VDD)	+25 V
Gate Voltage (VGG)	-5 to +1.5 V
Drain Current (IDD)	3.2A
Gate Current (IGG)	7mA
Input RF Power (Pin)*	30 dBm
Channel Temperature (Tch)	225°C
Mounting Temperature (30 seconds)	260°C

The operation of this device in excess of any of these limits may cause permanent damage.

* The max. input RF power, in principle, depends upon application frequency, matching circuit, and device voltage.

2.3 Recommended Operating Conditions

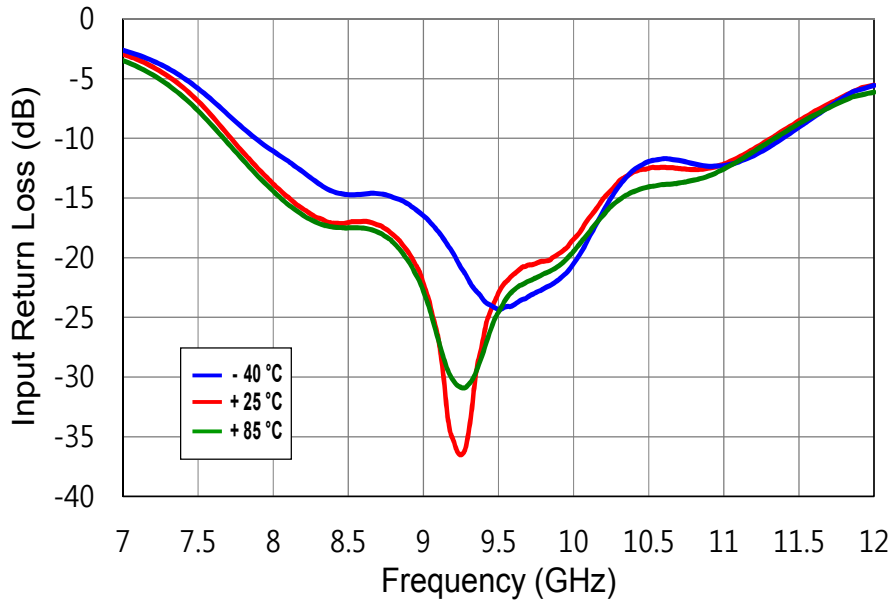
Parameters	Value
Drain Voltage (VDD)	$\leq +24$ V
Quiescent Drain Current (IDQ)	300 mA

3. Plots of Performance

S-parameter

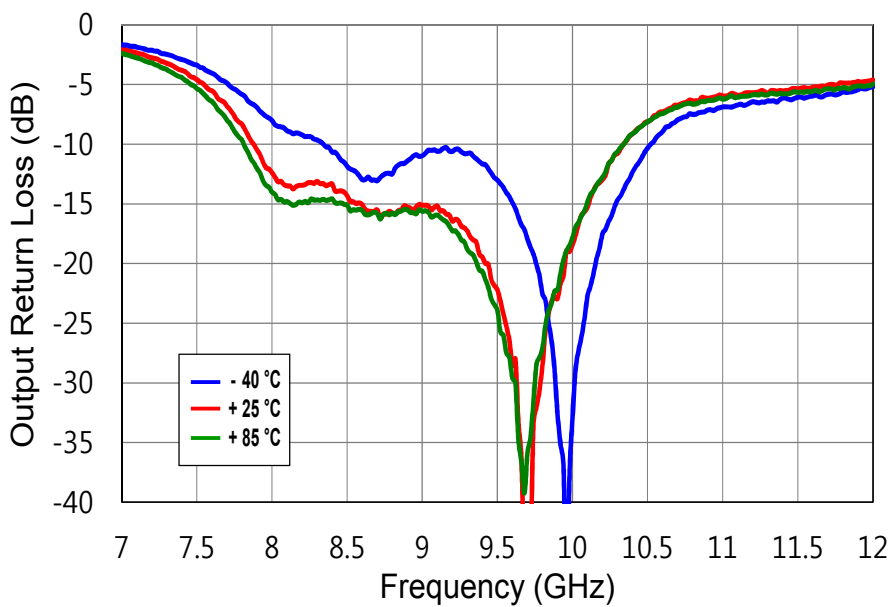
Input Return Loss vs. Frequency

VDD = +24 V, IDD = 300 mA, Pin = -30 dBm



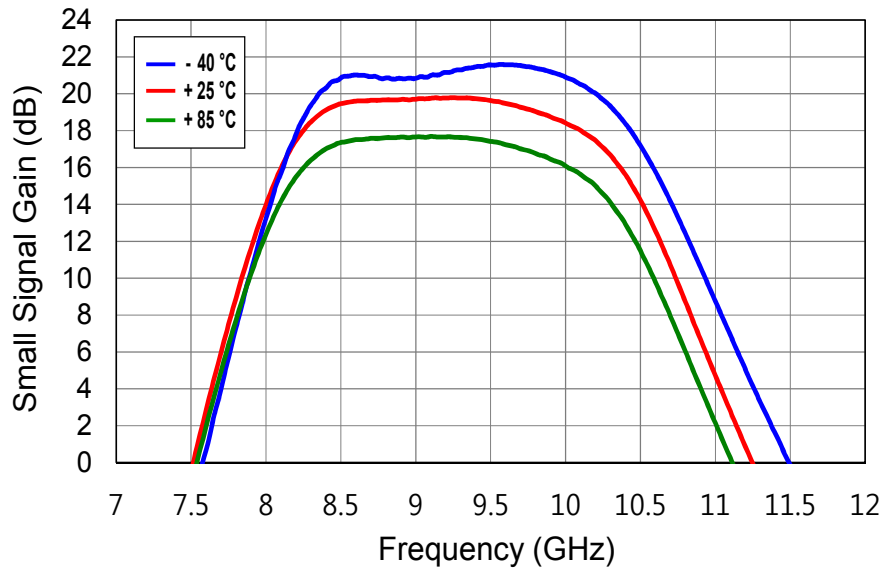
Output Return Loss vs. Frequency

VDD = +24 V, IDD = 300 mA, Pin = -30 dBm



Small Signal Gain vs. Frequency

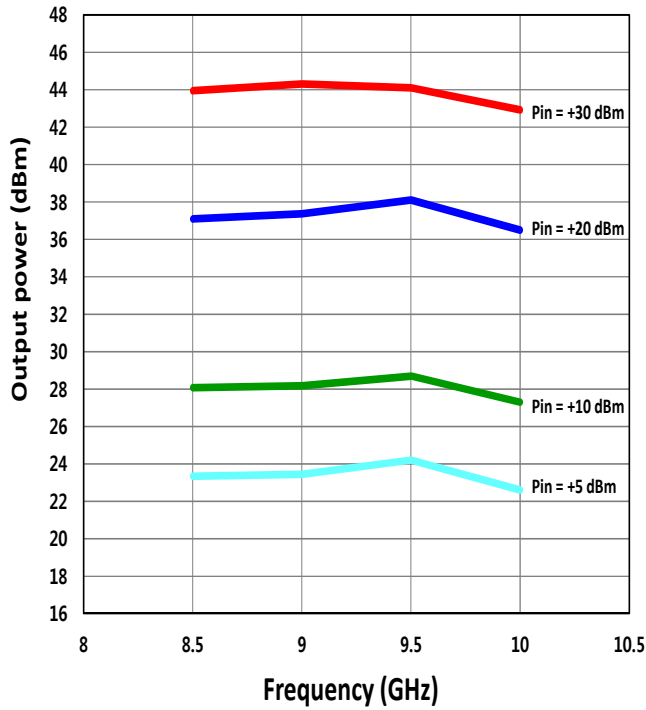
VDD = +24 V, IDD = 300 mA, Pin = -30 dBm



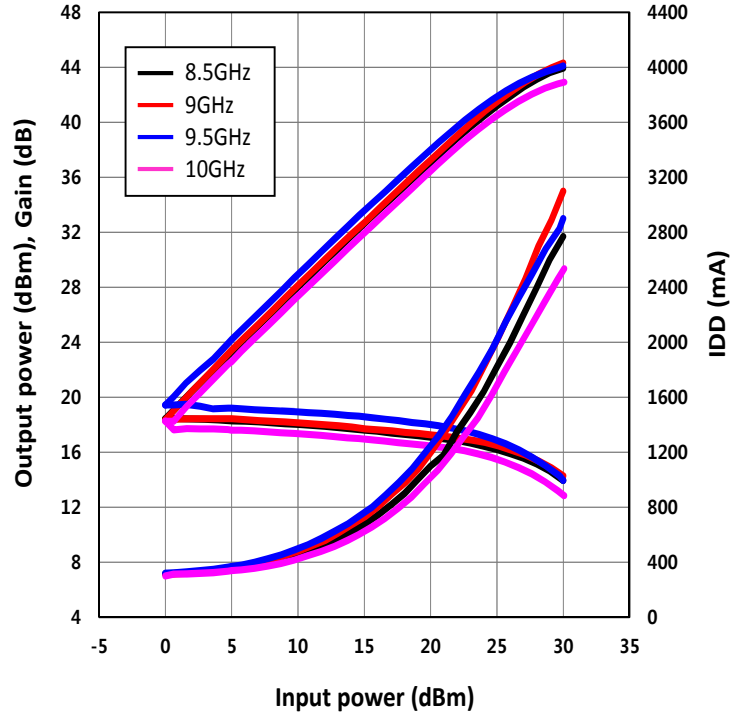
Typical Performance (Pulsed mode)

VDD = +24 V, IDD = 300 mA, Pulse width = 100 μ s, Duty Cycle = 10%

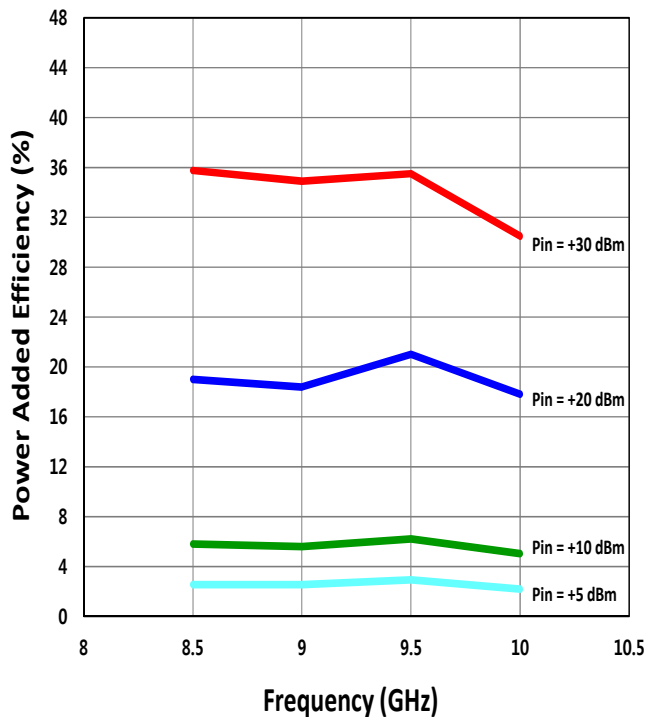
Output Power vs. Frequency



Output Power, Gain, IDD vs. Input Power



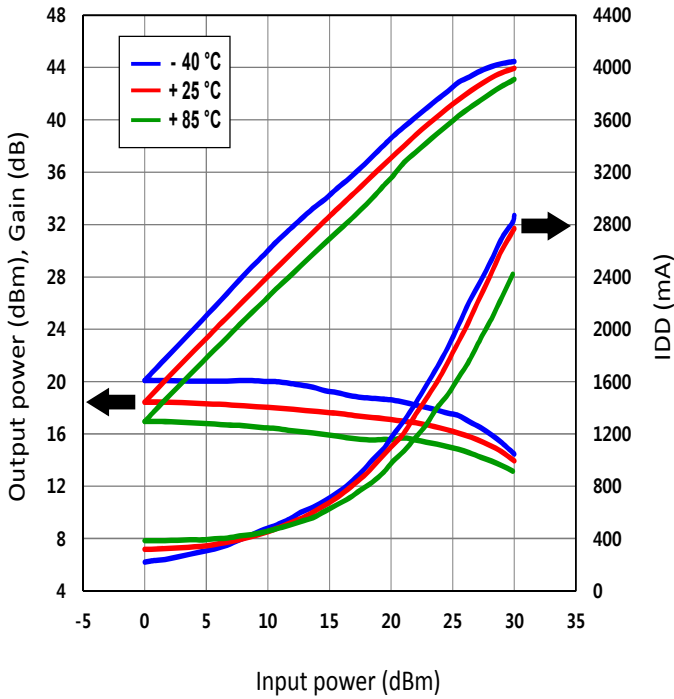
Power Added Efficiency vs. Frequency



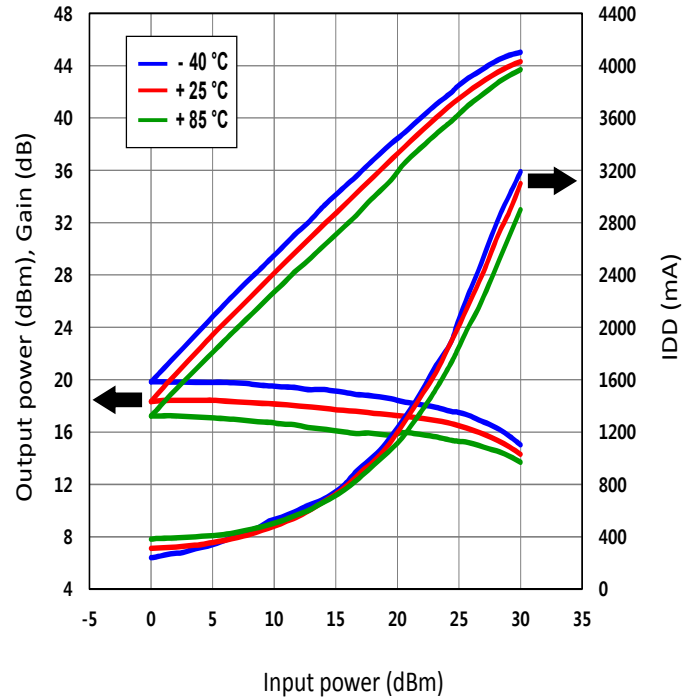
Output Power, Gain, IDD vs. Input Power (Pulsed mode)

VDD = +24 V, IDD = 300 mA, Pulse width = 100 μ s, Duty Cycle = 10%

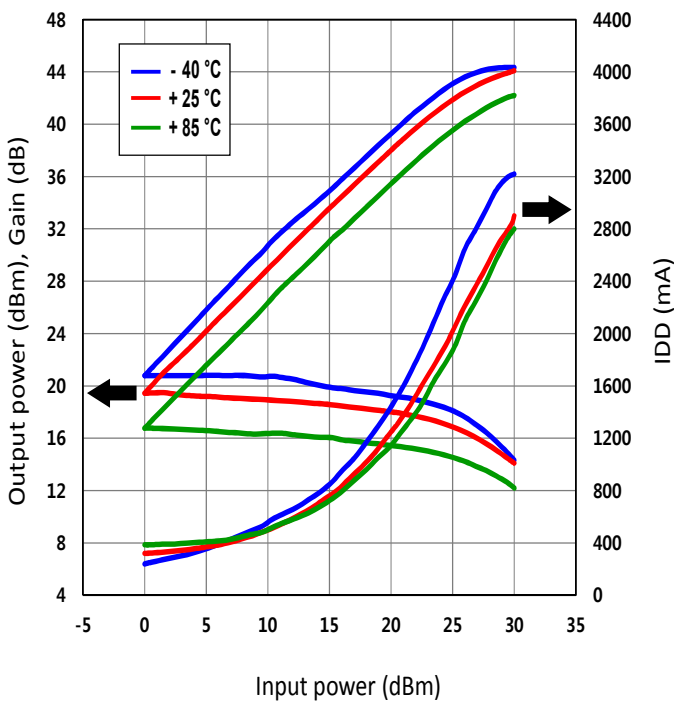
@ 8.5 GHz



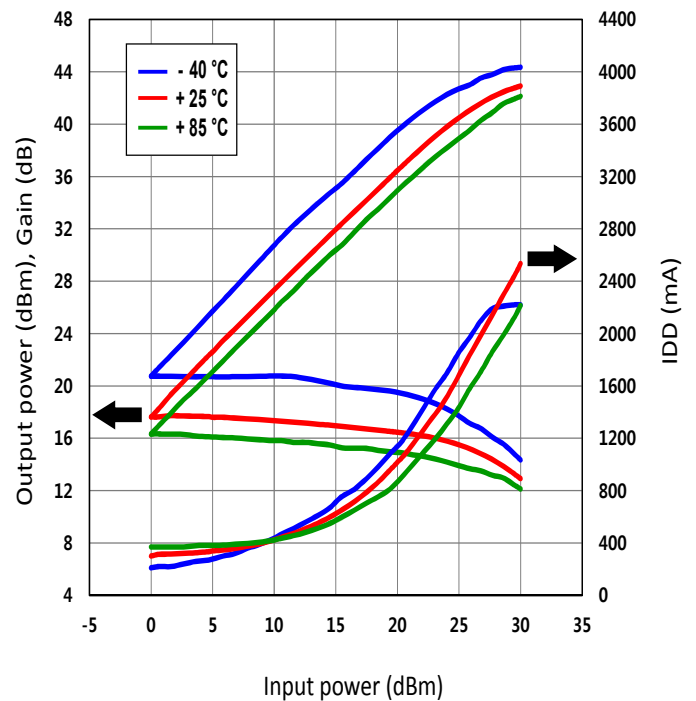
@ 9.0 GHz



@ 9.5 GHz



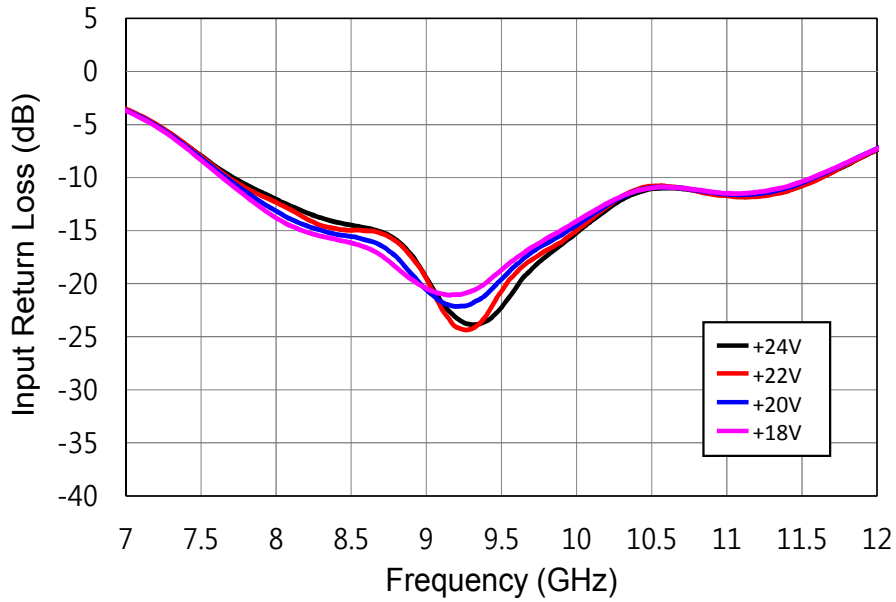
@ 10.0 GHz



S-parameter

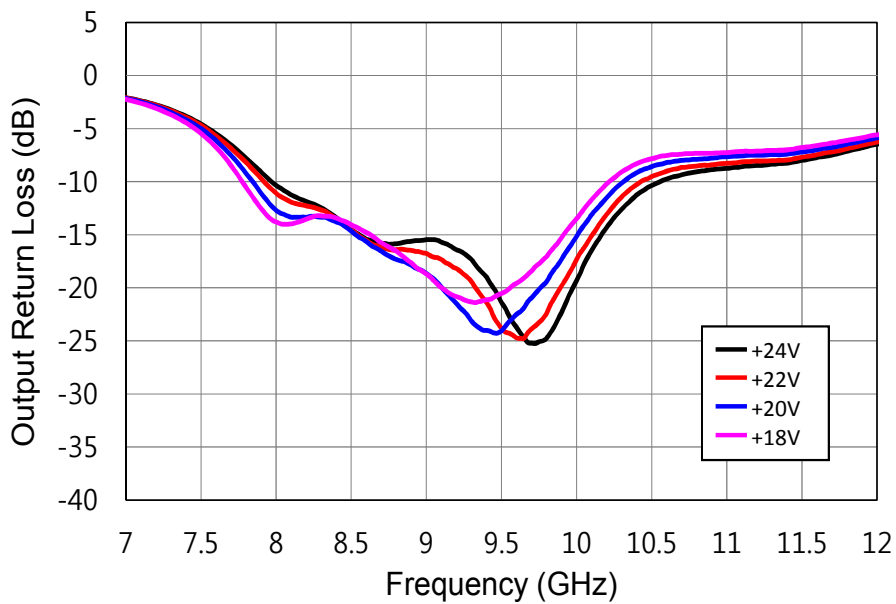
Input Return Loss vs. Frequency vs. VDD

IDD = 300 mA, Pin = -30 dBm



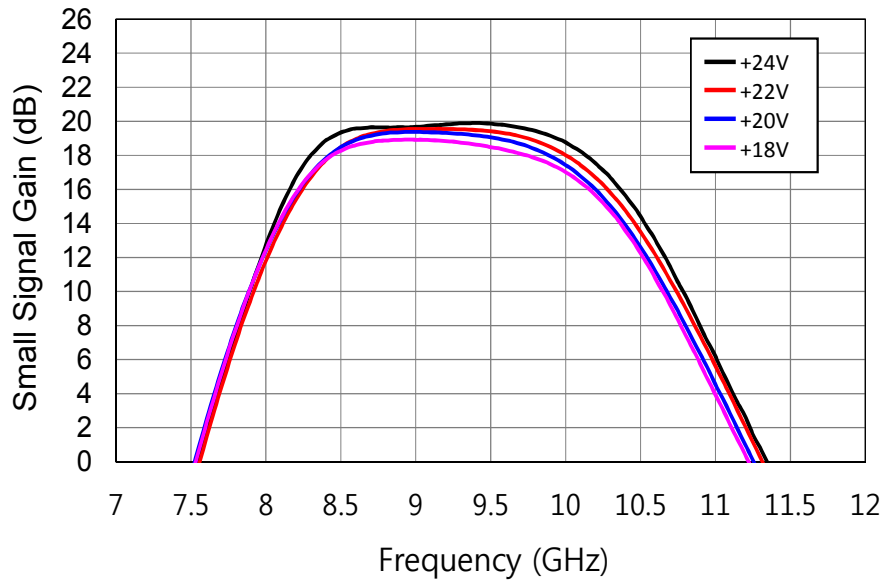
Output Return Loss vs. Frequency vs. VDD

IDD = 300 mA, Pin = -30 dBm



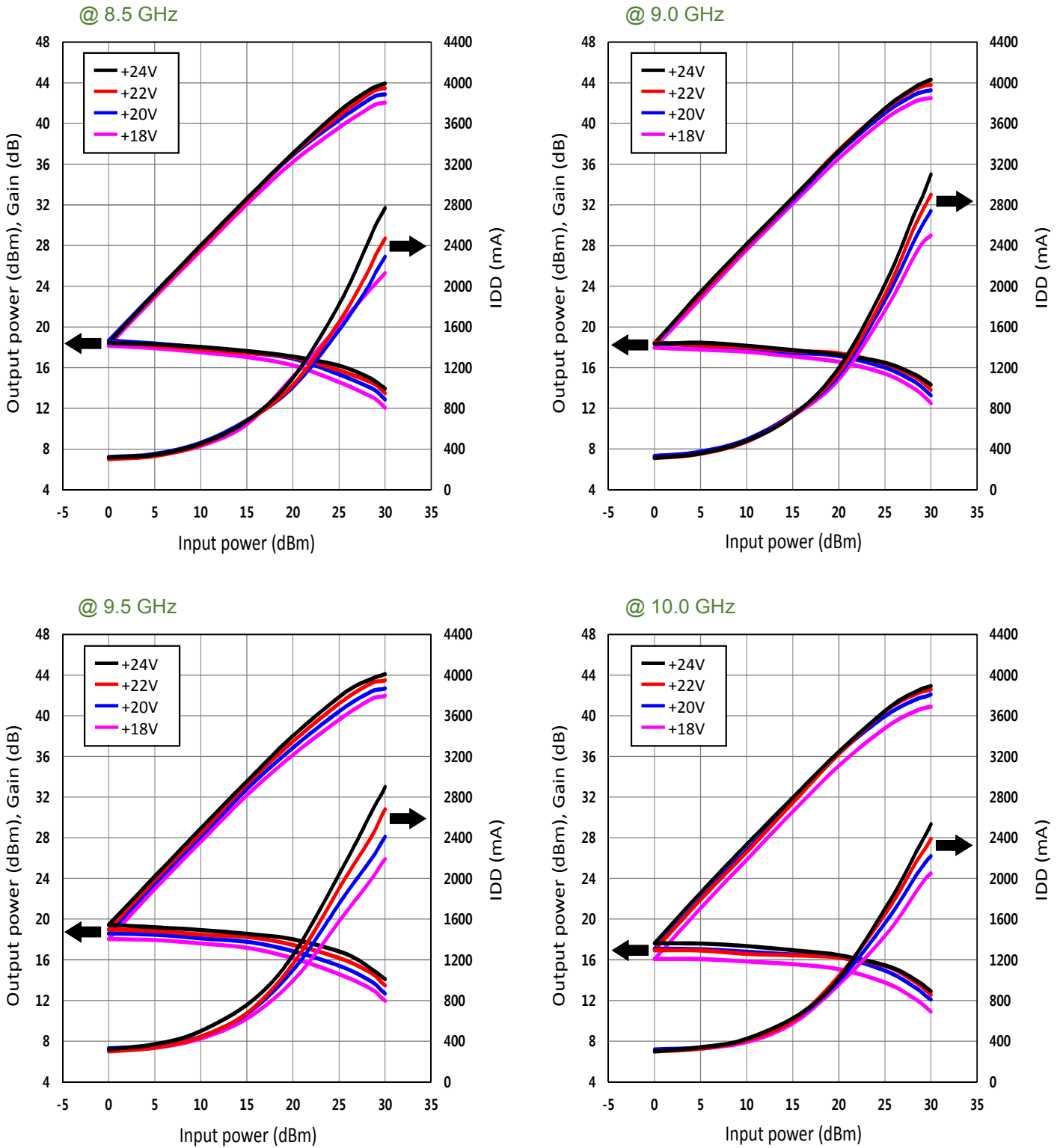
Small Signal Gain vs. Frequency vs. VDD

IDD = 300 mA, Pin = -30 dBm



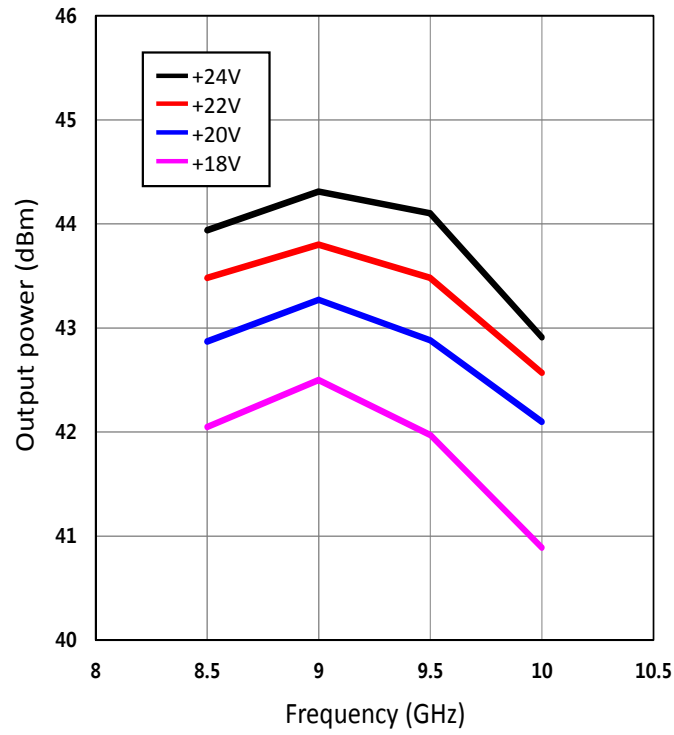
Output Power, Gain, IDD vs. Input Power vs. VDD (Pulsed mode)

IDD = 300 mA, Pulse width = 100 μ s, Duty Cycle = 10%



Output Power at Pin = 30 dBm vs. Frequency vs. VDD (Pulsed mode)

Pin = +30 dBm, Pulse width = 100 μ sec, Duty cycle = 10%



4. Thermal and Reliability Information

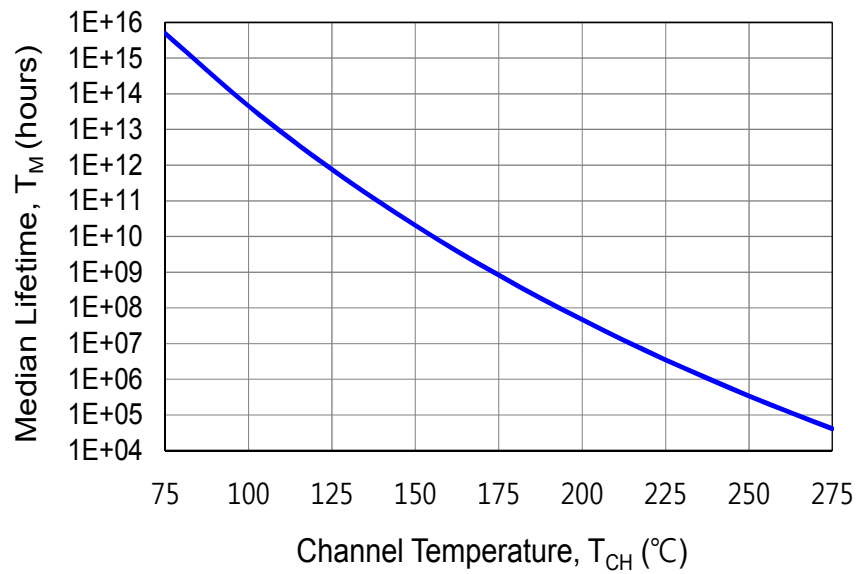
Parameters	Test Conditions	Value	Units
Thermal Resistance (θ_{JC}) ¹⁾	$T_{BASE} = 85^{\circ}C$, $V_D = +24 V$, $I_{DQ} = 300 mA$, CW, $P_{DISS} = 7.2 W$	4.5	$^{\circ}C/W$
Channel Temperature (T_{CH}) (Quiescent, No RF)		117	$^{\circ}C$
Median Lifetime (T_M)		2.5E+12	hours

1) Thermal resistance is measured to the package backside.

Median Lifetime

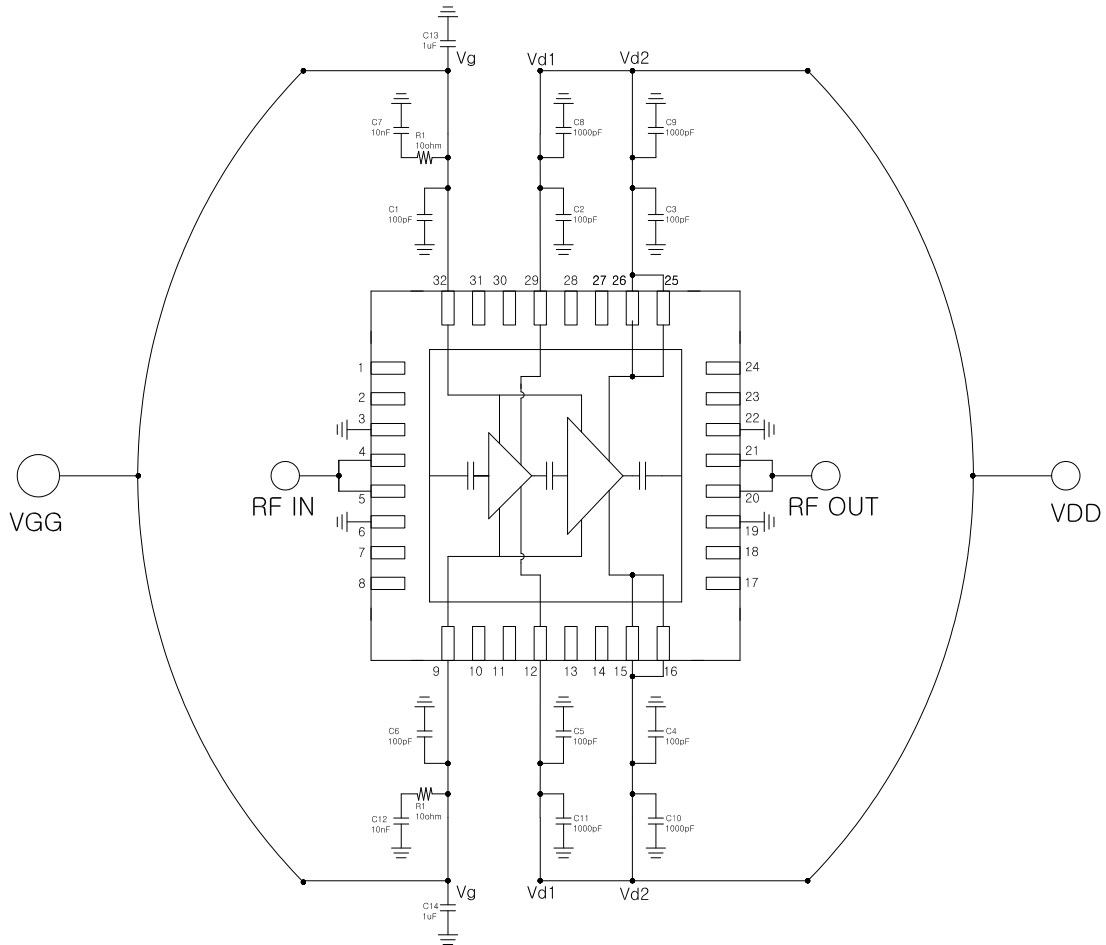
Median Life Test Conditions: $V_D = +28 V$, Failure Criteria = 20% reduction in I_{D_MAX} during DC Life Testing.

Median Lifetime vs. T_{CH}



5. Applications Information

5.1 Application Circuit



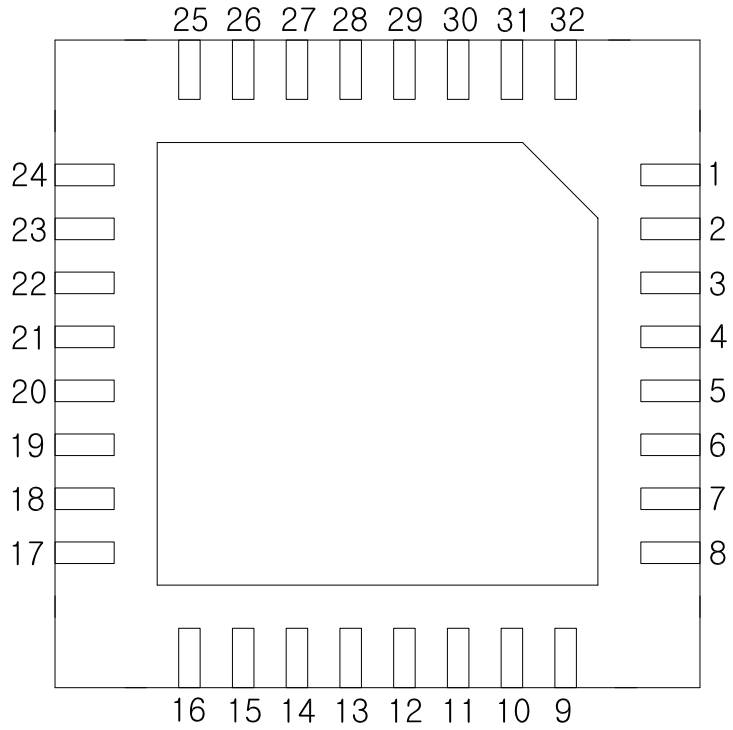
Note 1: The capacitors are recommended to be located close to the package.

5.2 Biasing Procedure

- Make sure no RF power is applied to the device before continuing.
- Pinch off device by setting VGG to -5 V.
- Raise VDD to +24 V while monitoring drain current.
- Raise VGG until drain current reaches 300 mA.
- Apply RF power.

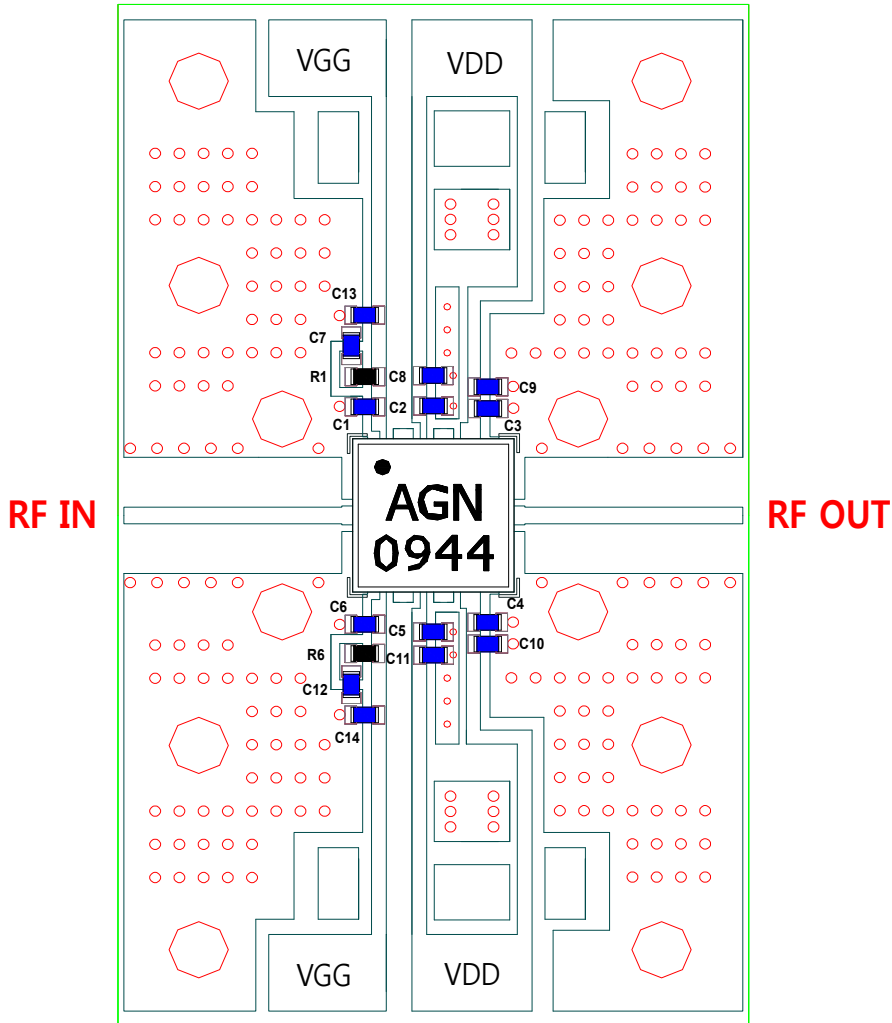
5.3 Pin Descriptions

Bottom View



Pin	Pin Name	Description
1, 2, 3, 6, 7, 8, 17, 18, 19, 22, 23, 24	GND	Must me grounded on the PCB
9, 32	Vg	Gate voltage
4, 5	RF IN	Input, matched to 50 ohms
13, 15, 16, 25, 26, 28, 30	Vd	Drain voltage
20, 21	RF OUT	Output, matched to 50 ohms
10, 14, 27, 31	NC	No internal connection

5.4 Evaluation Board Layout

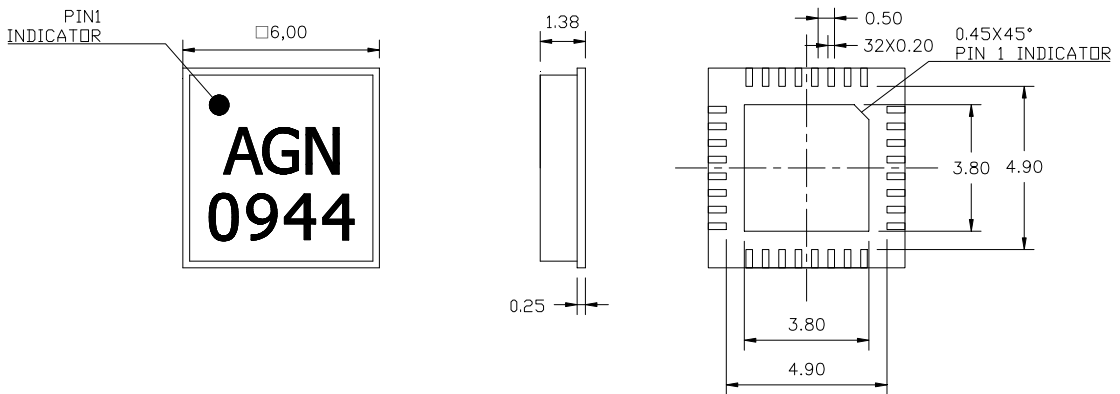


Bill of Materials

Reference Design	Value	Description	Manufacturer	Part Number
C1 - C6	100 pF	Cap, 1005	Various	
C7, C12	10 nF	Cap, 1005	Various	
C8, C9, C10, C11	1000 pF	Cap, 1005	Various	
C13, C14	1 μ F	Cap, 1005	Various	
R1 - R2	10 Ω	Res, 1005	Various	

5.5 Package Outline

Unit: mm



6. Product Compliance Information

6.1 Moisture Sensitivity Level (MSL)

Parameters	Rating	Standard
MSL-Convection Reflow 260°C	3	JEDEC standard IPC/JEDEC J-STD-020

(End of Datasheet)

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