AGN0942Q Data Sheet

X Band Power Amplifier MMIC

1. Product Overview

1.1 General Description

AGN0942Q is a two-stage internally matched MMIC Power Amplifier which operates between 8.5 GHz and 10 GHz frequency range. This product is well suited to X band applications. AGN0942Q is packaged in a 6x6 mm air-cavity QFN. This product is well suited to Point to Point Radio and Communications.

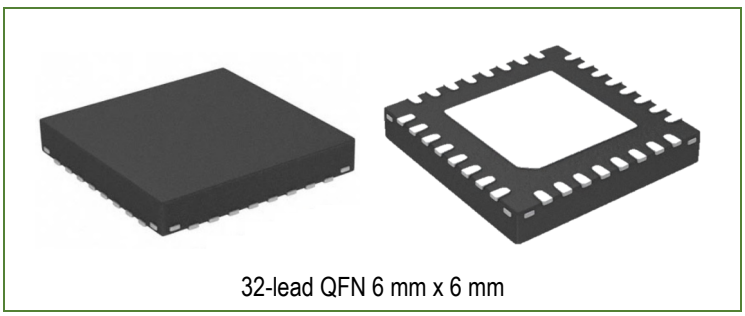
1.2 Features

- Frequency Range: 8.5 - 10 GHz
- Saturated Output Power: 41 dBm
- Power Added Efficiency: 35%
- Power Gain: 16 dB
- Small Signal Gain: 22 dB
- Bias: VDD = +24 V, IDD = 200 mA, VGG = -2.35 V (Typical)

1.3 Applications

- Point to Point Radio
- Communications

1.4 Package Profile



32-lead QFN 6 mm x 6 mm

2. Summary on Product Performances

2.1 Typical Performances (Pulsed mode)

Test conditions : T = +25°C, VDD = +24 V, Pulse width = 100 μs, Duty cycle = 10%.

Parameters	Test Conditions	Min	Typ	Max	Units
Gate Bias Voltage	*f* = 8.5 - 10 GHz		-2.35		V
Output Power at Psat[1)]	*f* = 8.5 - 10 GHz		41		dBm
Power Gain at Psat[1)]	*f* = 8.5 - 10 GHz		16		dB
Drain Current at Psat[1)]	*f* = 8.5 - 10 GHz		1800		mA
Power Added Efficiency at Psat[1)]	*f* = 8.5 - 10 GHz		35		%
Small Signal Gain	*f* = 8.5 - 10 GHz		22		dB
Input Return Loss	*f* = 8.5 - 10 GHz		-10		dB
Output Return Loss	*f* = 8.5 - 10 GHz		-10		dB
Drain Current			200		mA

1) Psat: Saturated output power

2.2 Absolute Maximum Ratings (not simultaneous) at 25˚C

Parameters	Max. Ratings
Operating Case Temperature (Tc)	-40 to +85°C
Storage Temperature (Tstg)	-55 to +125°C
Drain Voltage (VDD)	+25 V
Gate Voltage (VGG)	-5 to -1.5V
Drain Current (IDD)	1.8A
Gate Current (IGG)	5mA
Input RF Power (Pin)*	25 dBm
Channel Temperature (T_{CH})	225°C
Mounting Temperature (30 seconds)	260°C

The operation of this device in excess of any of these limits may cause permanent damage.
* The max. input RF power, in principle, depends upon application frequency, matching circuit, and device voltage.

2.3 Recommended Operating Conditions

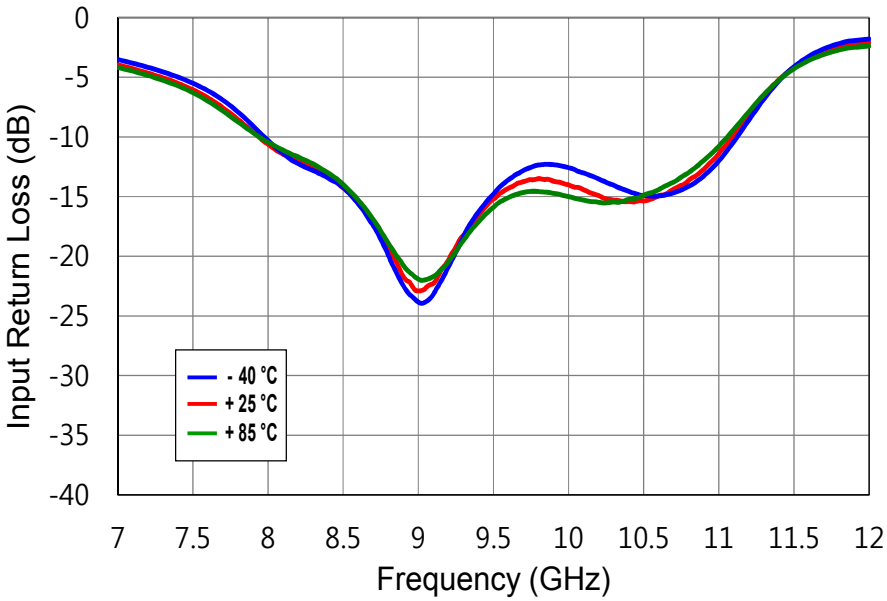
Parameters	Value
Drain Voltage (VDD)	<=+24 V
Quiescent Drain Current (IDQ)	200 mA

3. Plots of Performance

S-parameter

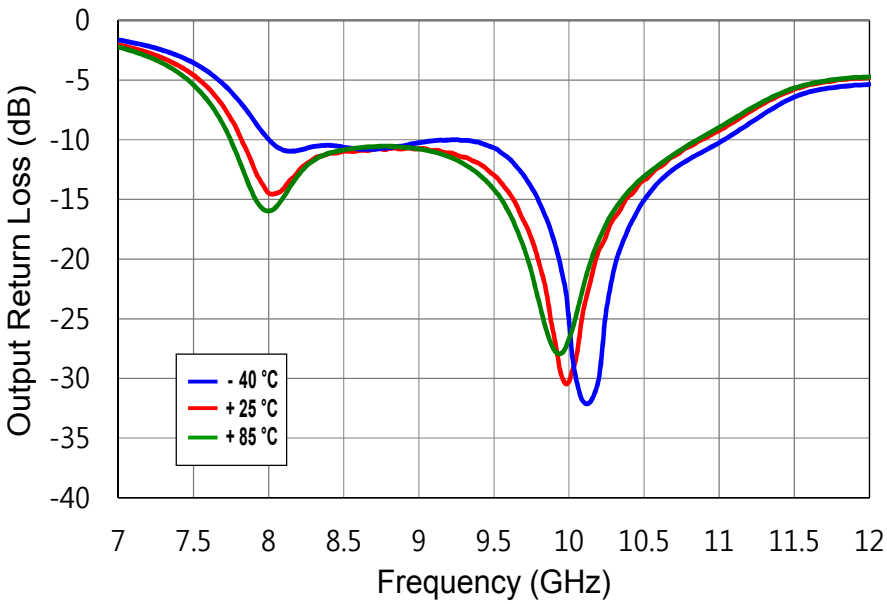
Input Return Loss vs. Frequency vs. Temp

VDD = +24 V, IDD = 200 mA, Pin = -30 dBm



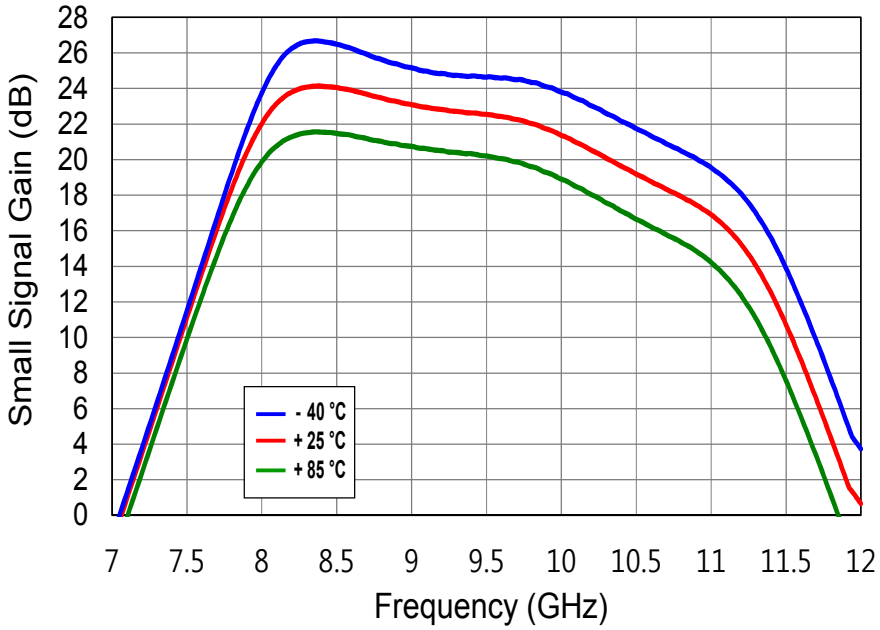
Input Return Loss vs. Frequency vs. Temp

VDD = +24 V, IDD = 200 mA, Pin = -30 dBm



Small Signal Gain vs. Frequency vs. Temp

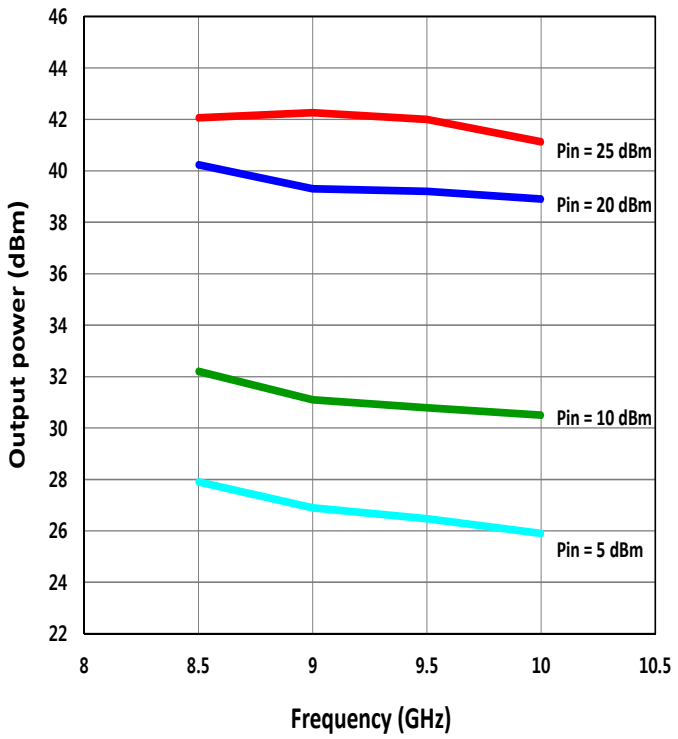
VDD = +24 V, IDD = 200 mA, Pin = -30 dBm



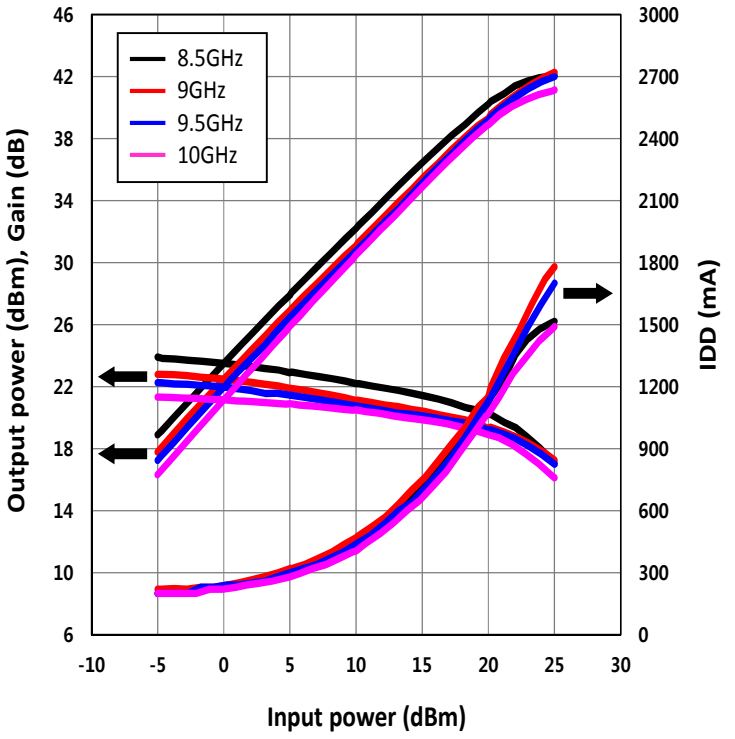
Typical Performance (Pulsed mode)

VDD = +24 V, IDD = 200 mA, Pulse width = 100 μs, Duty Cycle = 10%

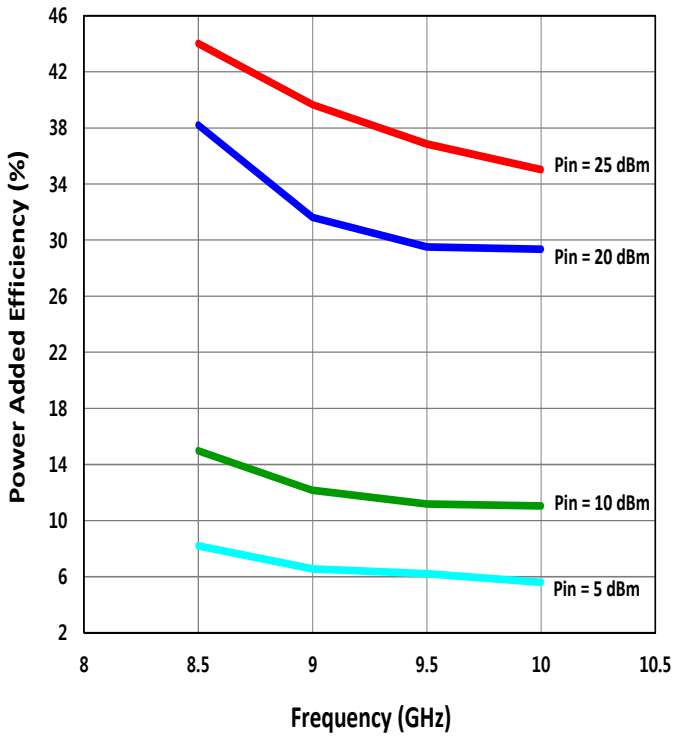
Output Power vs. Frequency vs. Pin



Output Power, Gain, IDD vs. Input Power vs. Frequency



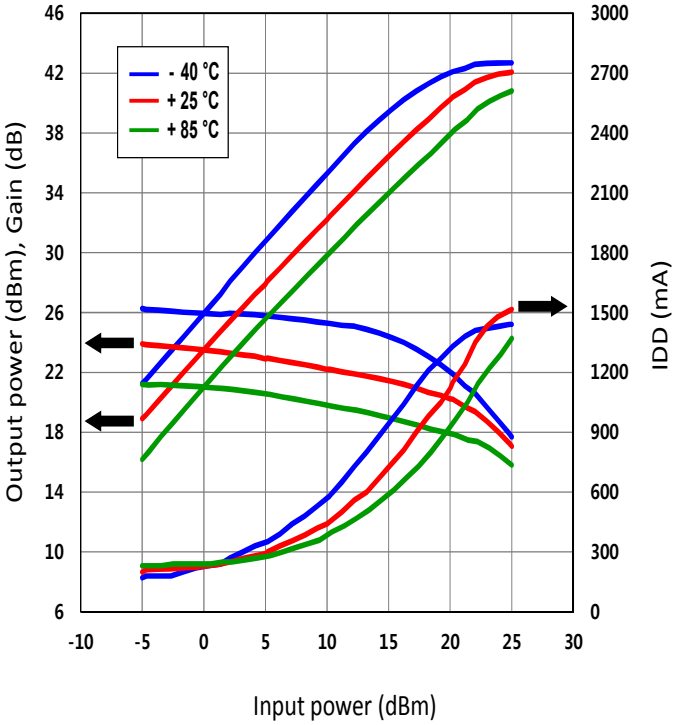
Power Added Efficiency vs. Frequency vs. Pin



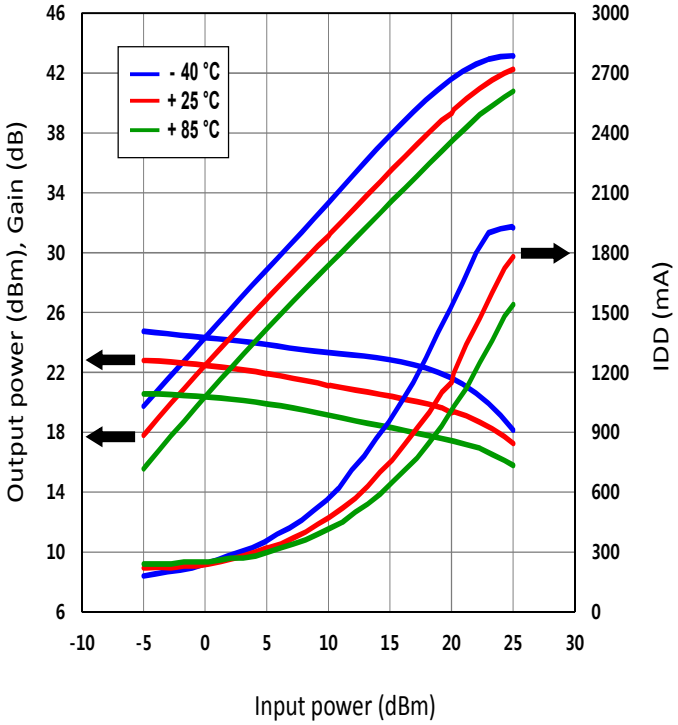
Output Power, Gain, IDD vs. Input Power vs. Temp (Pulsed mode)

VDD = +24 V, IDD = 200 mA, Pulse width = 100 μs, Duty Cycle = 10%

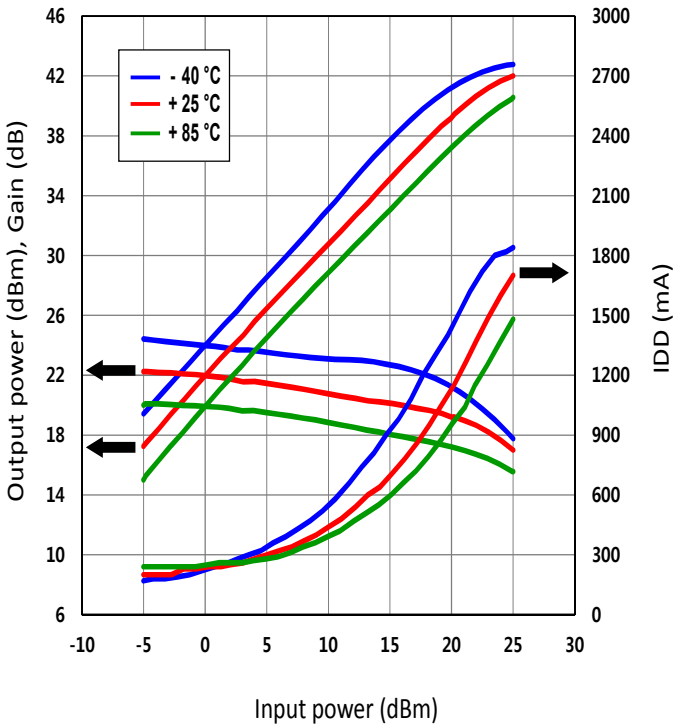
@ 8.5 GHz



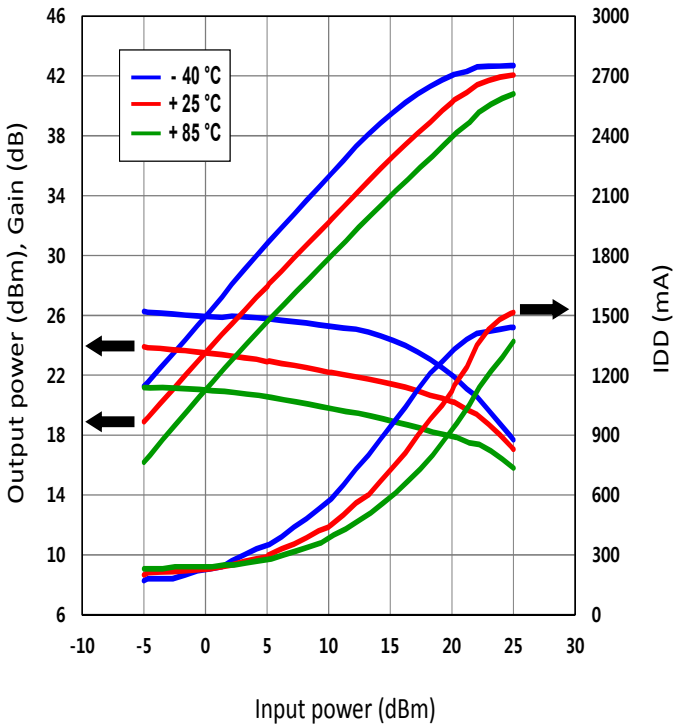
@ 9.0 GHz



@ 9.5 GHz



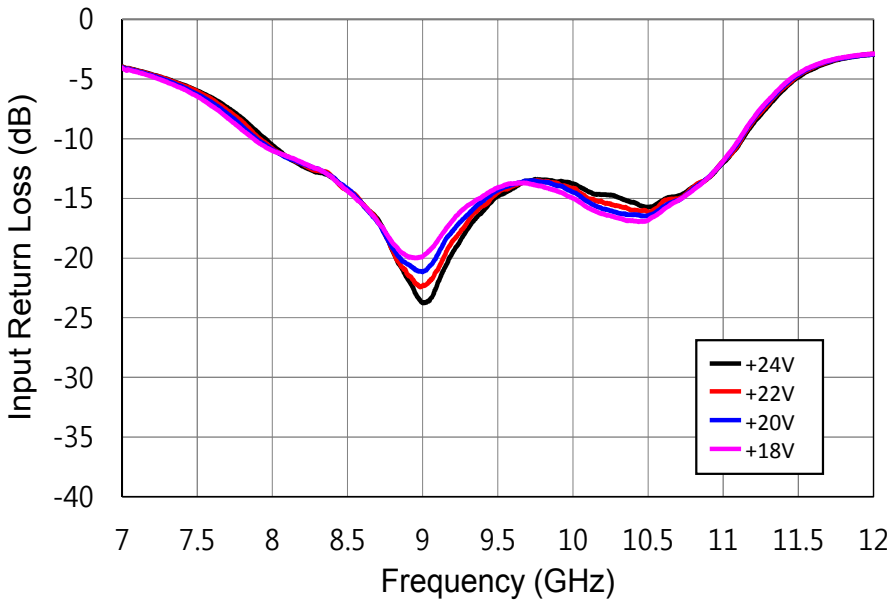
@ 10.0 GHz



S-parameter

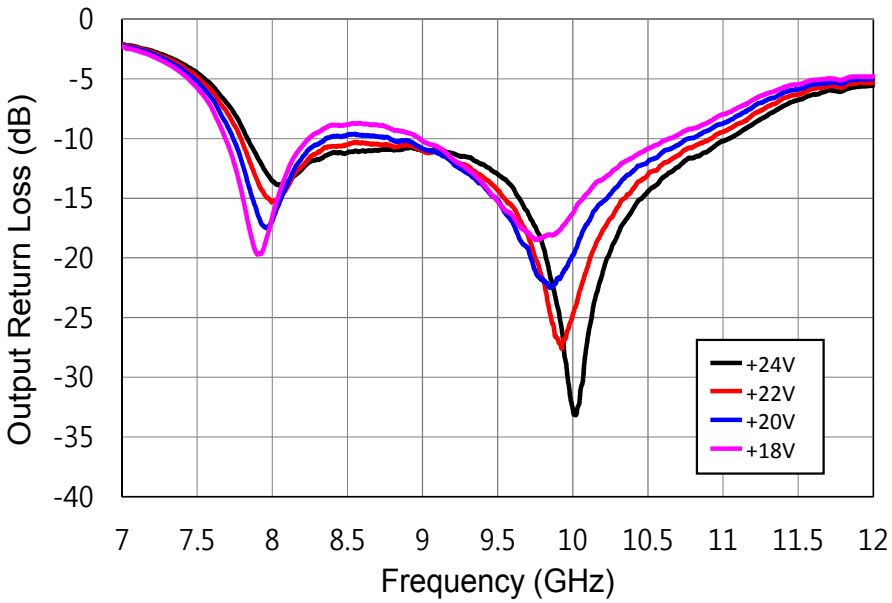
Input Return Loss vs. Frequency vs. VDD

IDD = 200 mA, Pin = -30 dBm



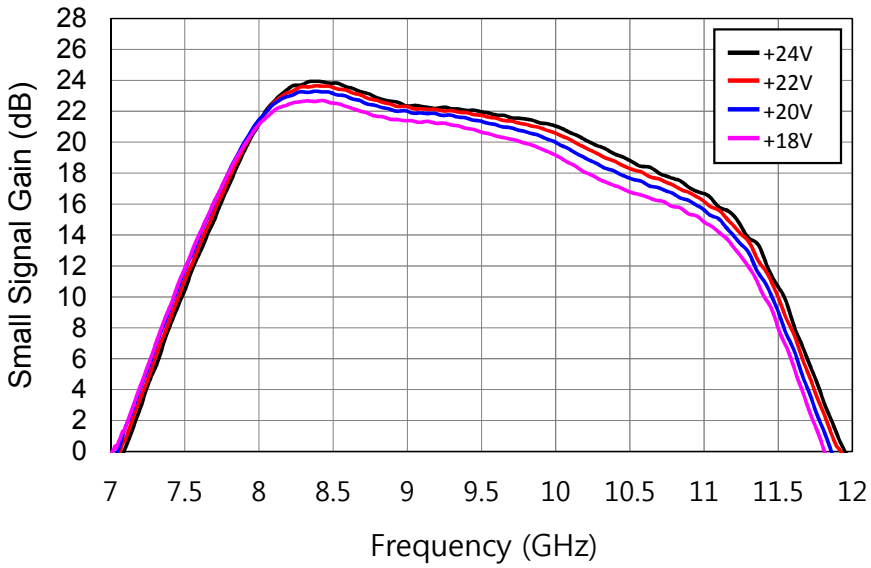
Output Return Loss vs. Frequency vs. VDD

IDD = 200 mA, Pin = -30 dBm



Small Signal Gain vs. Frequency vs. VDD

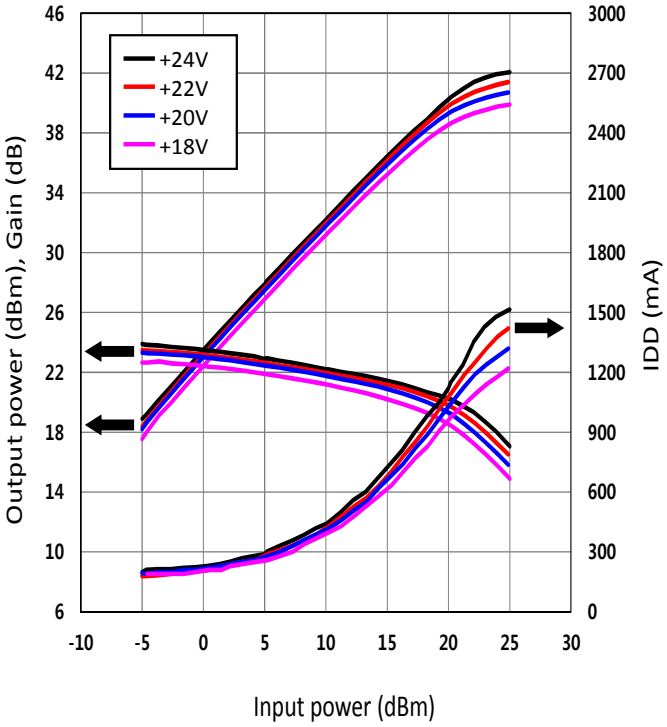
IDD = 200 mA, Pin = -30 dBm



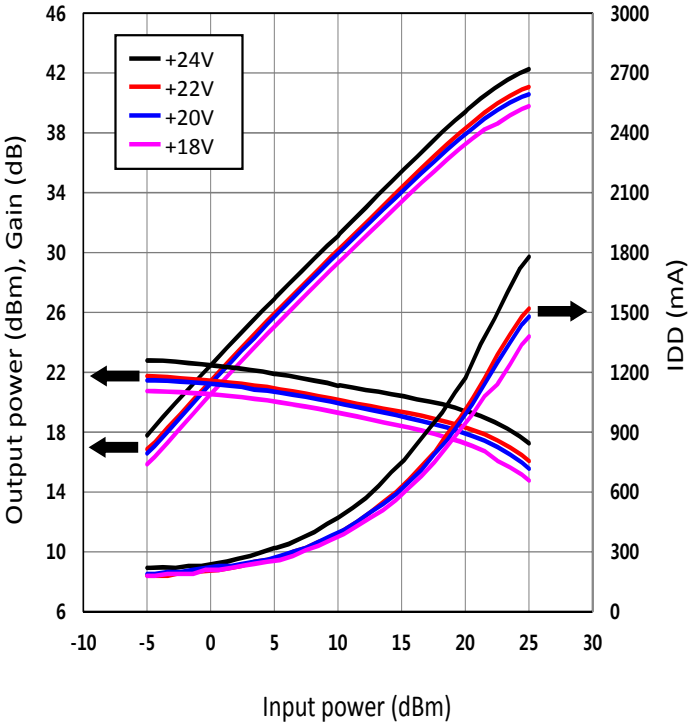
Output Power, Gain, IDD vs. Input Power vs. VDD (Pulsed mode)

IDD = 200 mA, Pulse width = 100 μs, Duty Cycle = 10%

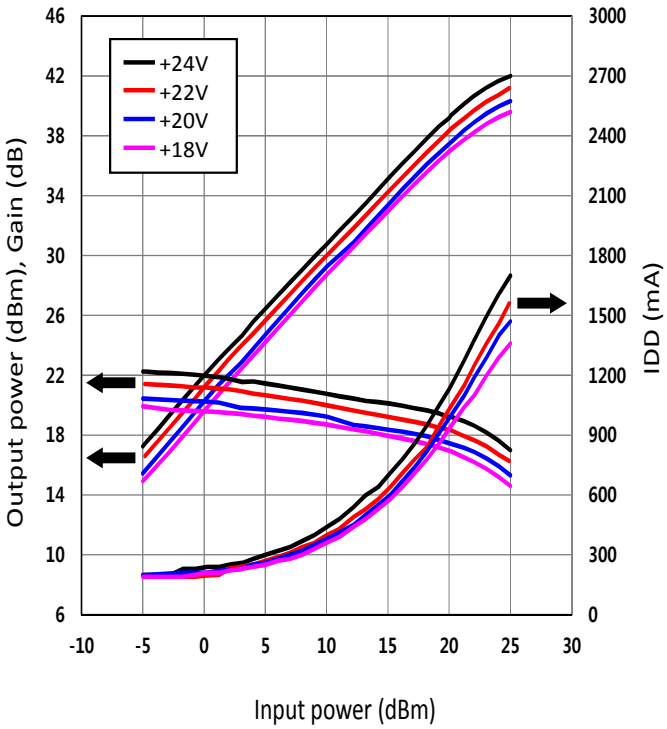
@ 8.5 GHz



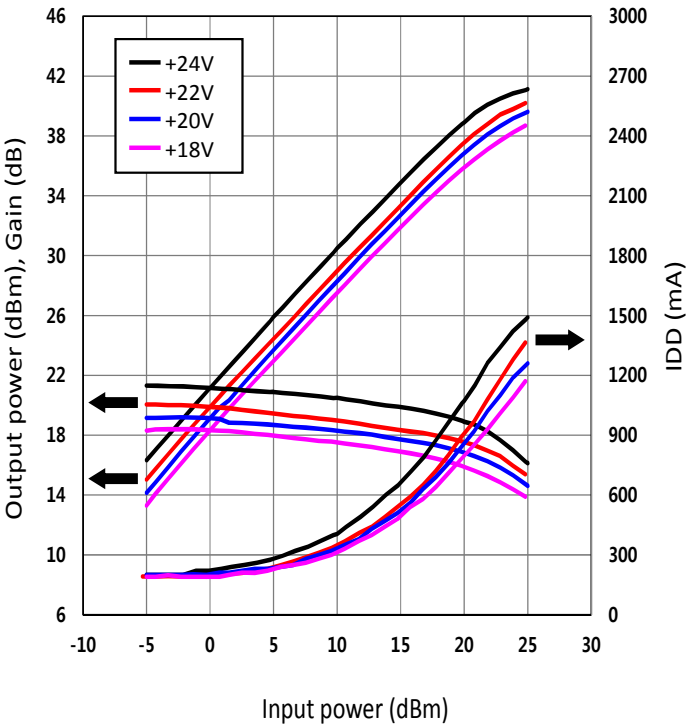
@ 9.0 GHz



@ 9.5 GHz

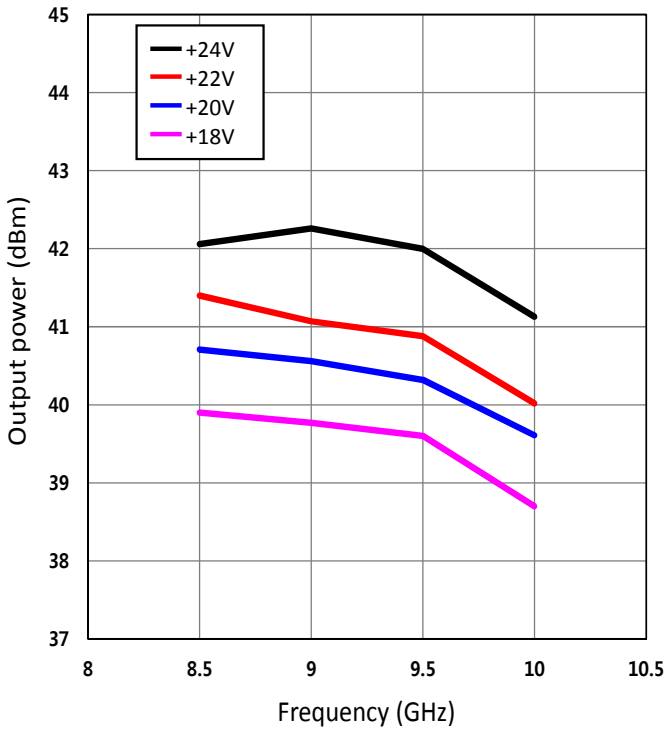


@ 10.0 GHz



Output Power at Pin = 25dBm vs. Frequency vs. VDD (Pulsed mode)

Pin = +25 dBm, Pulse width = 100 μsec, Duty cycle = 10%



4. Thermal and Reliability Information

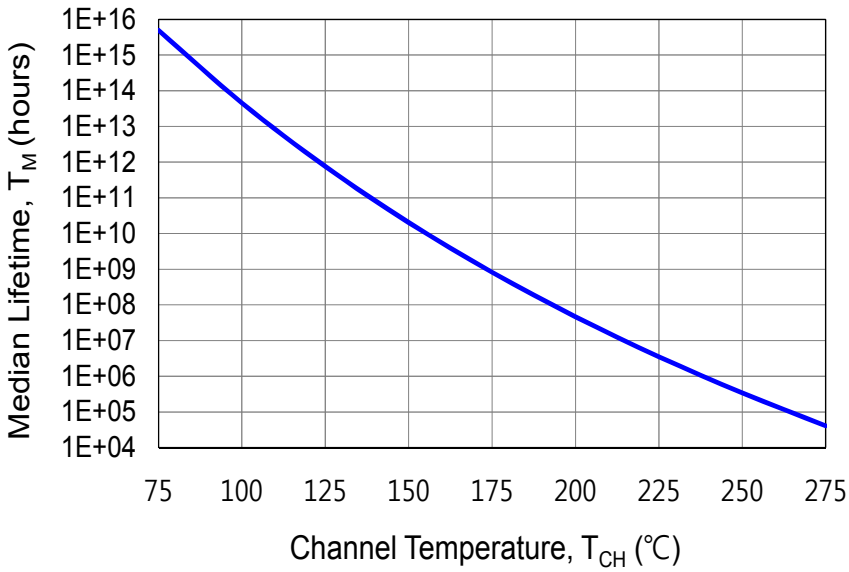
Parameters	Test Conditions	Value	Units
Thermal Resistance (θ_{JC})[1)]	T_{BASE} = 85°C, V_D = +24 V, I_{DQ} = 200 mA, CW, P_{DISS} = 4.8 W	7.8	°C/W
Channel Temperature (T_{CH}) (Quiescent, No RF)		122	°C
Median Lifetime (T_M)		1.1E+12	hours

1) Thermal resistance is measured to the package backside.

Median Lifetime

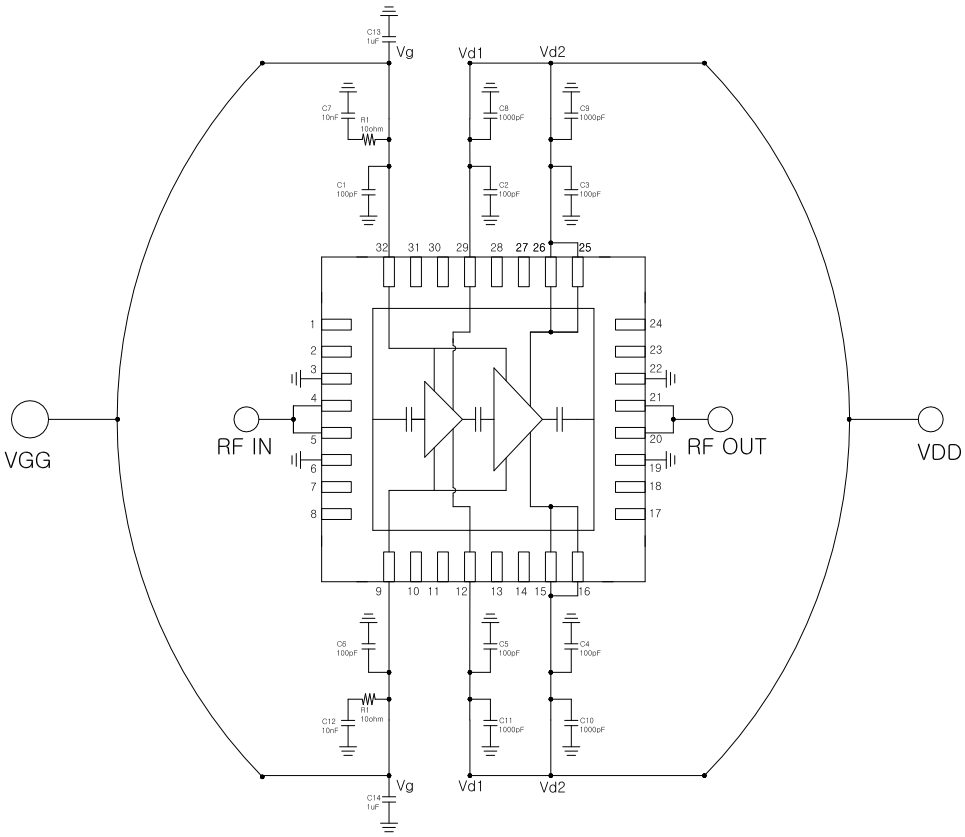
Median Life Test Conditions: V_D = +28 V, Failure Criteria = 20% reduction in I_{D_MAX} during DC Life Testing.

Median Lifetime vs. T_{CH}



5. Applications Information

5.1 Application Circuit



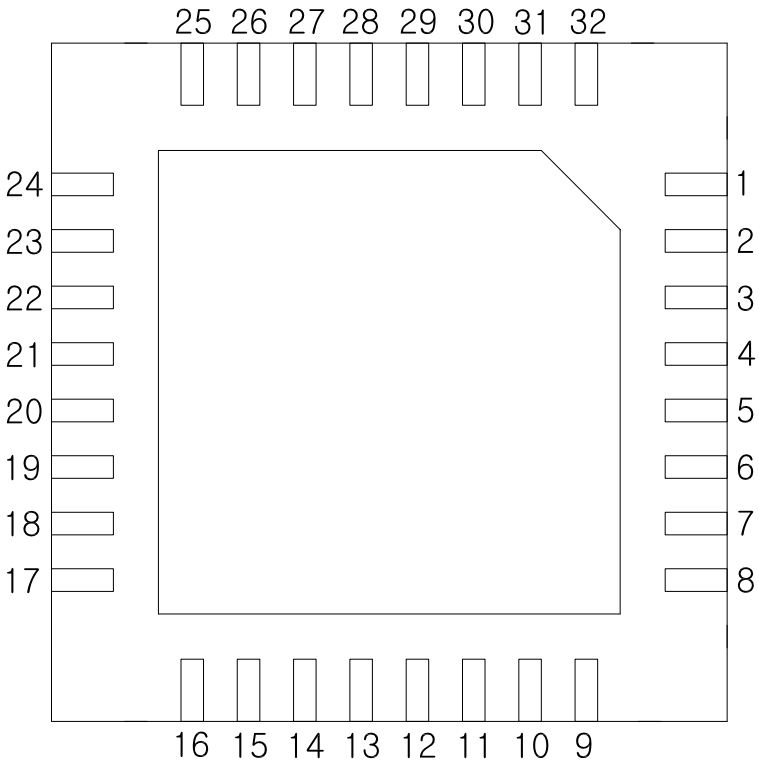
Note 1: The capacitors are recommended to be located close to the package.

5.2 Biasing Procedure

- Make sure no RF power is applied to the device before continuing.
- Pinch off device by setting VGG to -5 V.
- Raise VDD to +24 V while monitoring drain current.
- Raise VGG until drain current reaches 200 mA.
- Apply RF power.

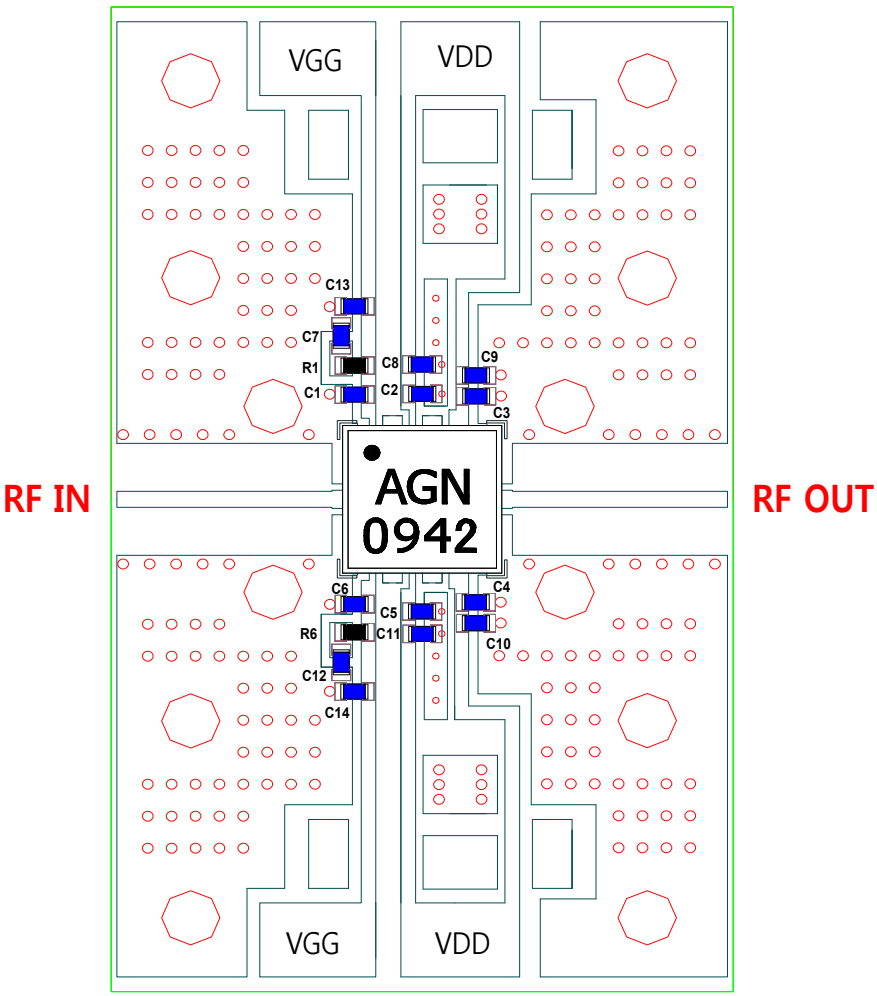
5.3 Pin Descriptions

Bottom View



Pin	Pin Name	Description
1, 2, 3, 6, 7, 8, 17, 18, 19, 22, 23, 24	GND	Must me grounded on the PCB
9, 32	Vg	Gate voltage
4, 5	RF IN	Input, matched to 50 ohms
13, 15, 16, 25, 26, 28, 30	Vd	Drain voltage
20, 21	RF OUT	Output, matched to 50 ohms
10, 14, 27, 31	NC	No internal connection

5.4 Evaluation Board Layout

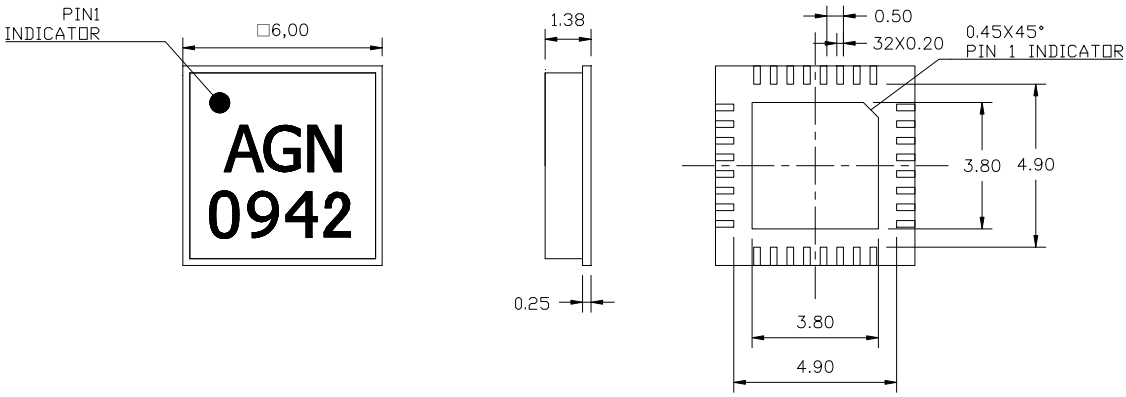


Bill of Materials

Reference Design	Value	Description	Manufacturer	Part Number
C1 - C6	100 pF	Cap, 1005	Various	
C7, C12	10 nF	Cap, 1005	Various	
C8, C9, C10, C11	1000 pF	Cap, 1005	Various	
C13, C14	1 μF	Cap, 1005	Various	
R1 - R2	10Ω	Res, 1005	Various	

5.5 Package Outline

Unit: mm



6. Product Compliance Information

6.1 Moisture Sensitivity Level (MSL)

Parameters	Rating	Standard
MSL-Convection Reflow 260℃	3	JEDEC standard IPC/JEDEC J-STD-020

(End of Datasheet)