Preliminary datasheet for X-band CMOS Core Chip

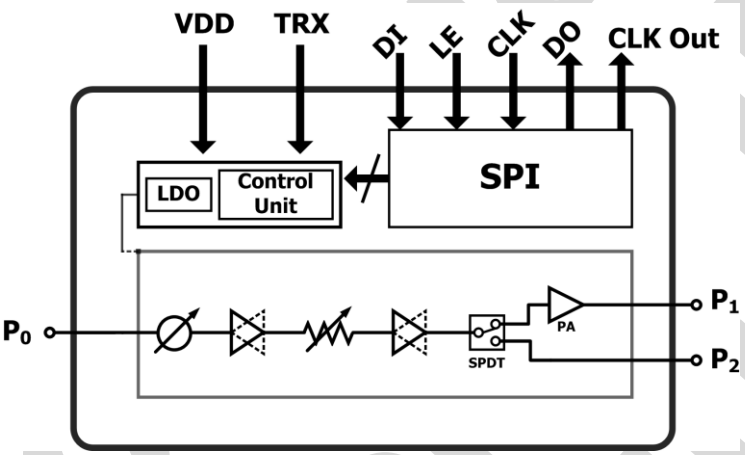
Rev 03-JUN.-14

Description

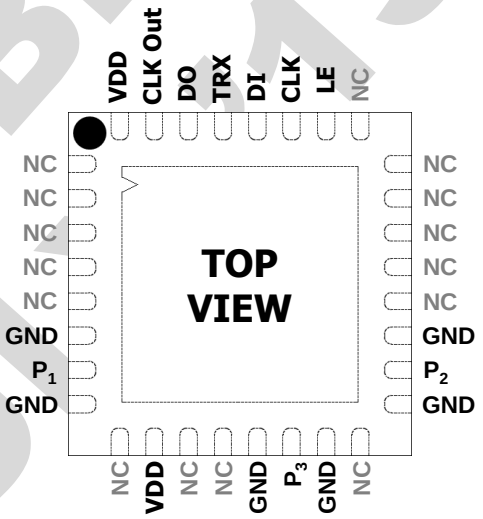
RMF080100PA is a QFN packaged X-band core chip which includes 6-bit phase shifter, 5-bit attenuator, 6-bit tuning circuits, bidirectional gain blocks (BDGB), medium power amplifier (MPA), low dropout regulator (LDO), and serial to parallel interface (SPI). It covers frequency range from 8 GHz to 10 GHz, phase shifting range 360° with 5.625° step, and attenuation range 31 dB with 1dB step. This device is fabricated in CMOS process.

Features

- 6-Bit Digital Phase Shifter
- 5-Bit Digital Attenuator
- 6-Bit Tuning Circuits (phase and amplitude)
- LSB=5.625°, 1dB
- 360 °, 31 dB coverage
- Power consumption:
  830mW (TX mode), 330mW (RX mode)
- Package Size 5 x 5 x 1 mm^3, 32 leads



Block diagram of the X-band Core Chip



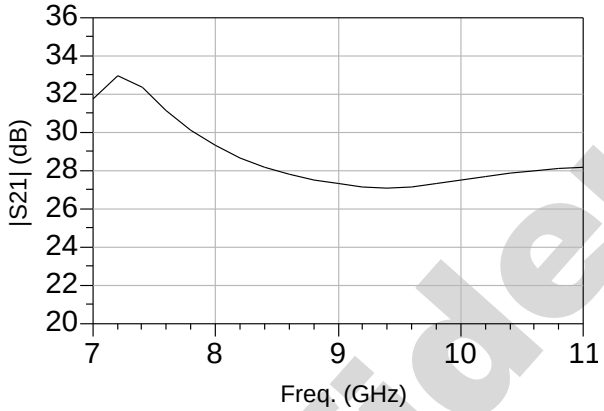
Pin configuration

Main Characteristics (T_{amb}=25 °C)

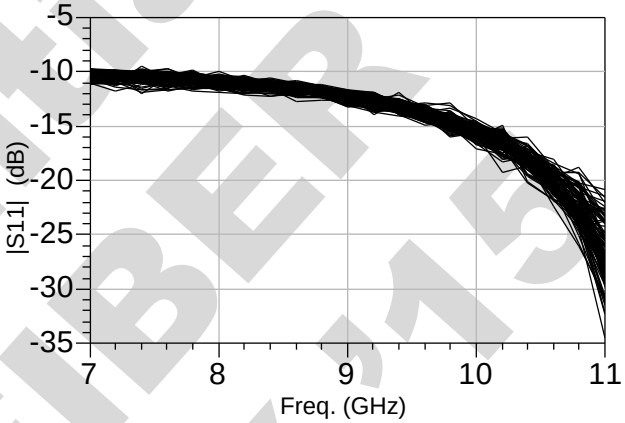
Parameter	MIN.	TYP.	MAX.
Operation Frequency (GHz)	8		10
Tx mode linear gain |S21| (dB)		27	
Rx mode linear gain |S13| (dB)		7	
RMS Attenuation Error (dB)		0.5	
RMS Phase Error (°)		1.5	
Output P1 dB in TX mode (dBm)		14	
Input P1 dB in RX mode (dBm)		-5	
SPI Clock Frequency (MHz)		50	

S-parameters and large signal performance in TX mode

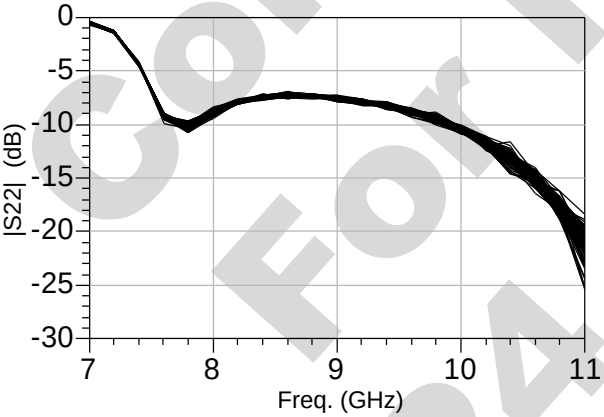
Small Signal Gain
(phase shifter state=ref., attenuator state=ref. ,T_{amb}=25°C)



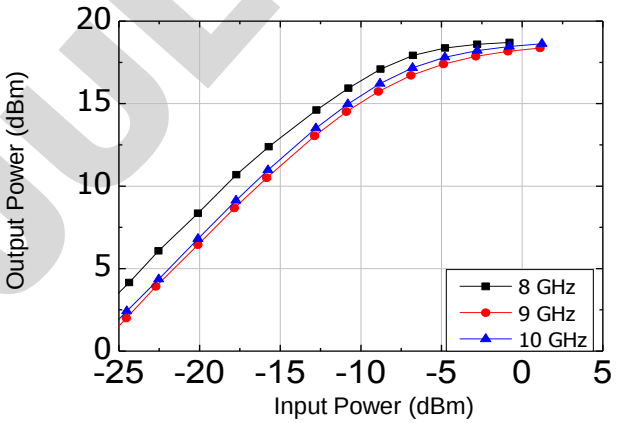
Port1 Return Loss
(for all attenuator and phase shifter states, T_{amb}=25°C)



Port2 Return Loss
(for all attenuator and phase shifter states, T_{amb}=25°C)

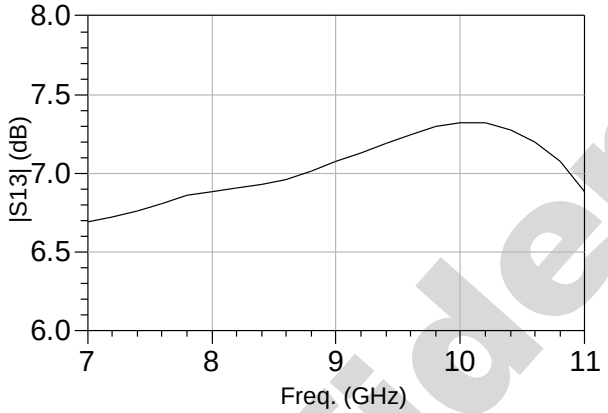


Output Power at Port2
(phase shifter state=ref., attenuator state=ref., T_{amb}=25°C)

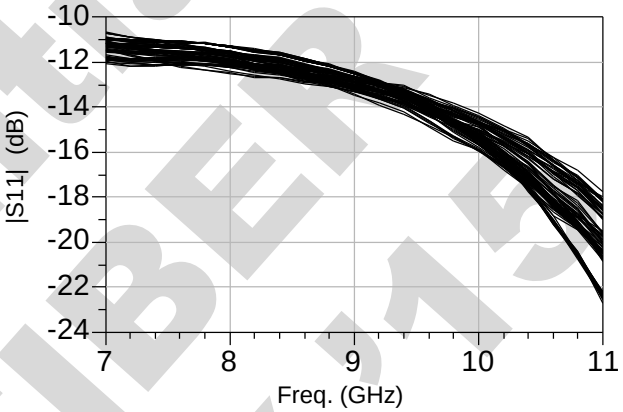


S-parameters in RX mode

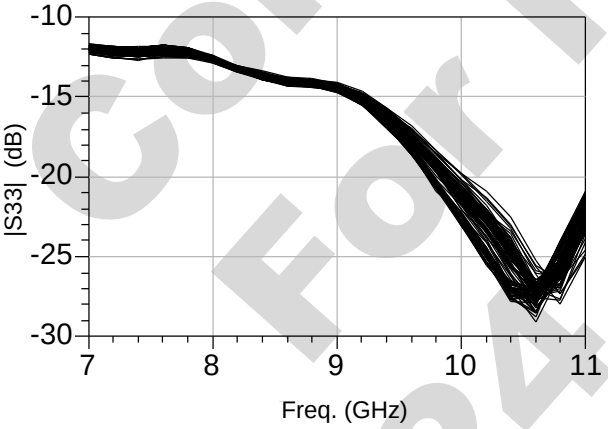
Small Signal Gain
(phase shifter state=ref., attenuator state=ref. ,T_{amb}=25°C)



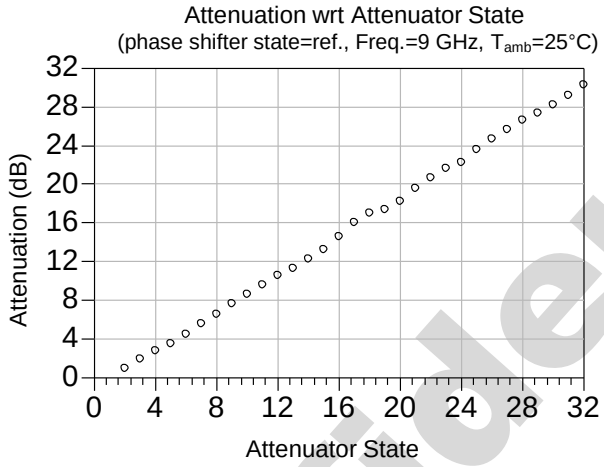
Port1 Return Loss
(for all attenuator and phase shifter states, T_{amb}=25°C)

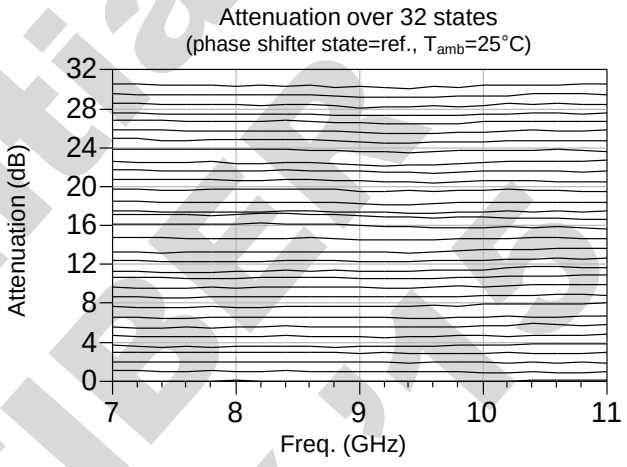


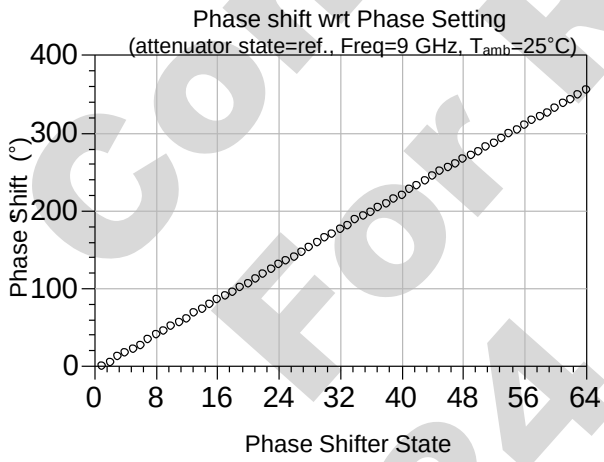
Port3 Return Loss
(for all attenuator and phase shifter states, T_{amb}=25°C)

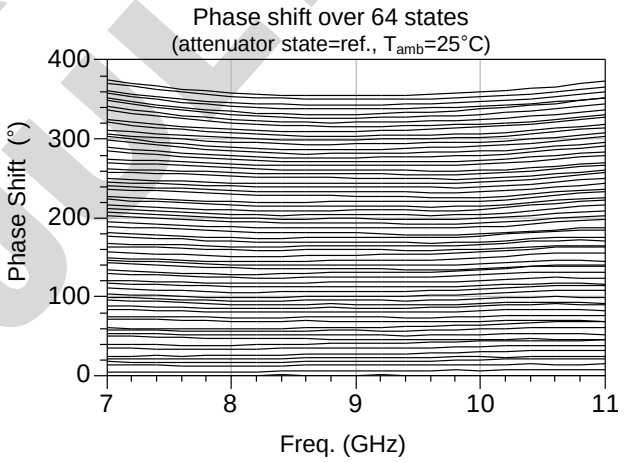


Attenuator and Phase Shifter Response



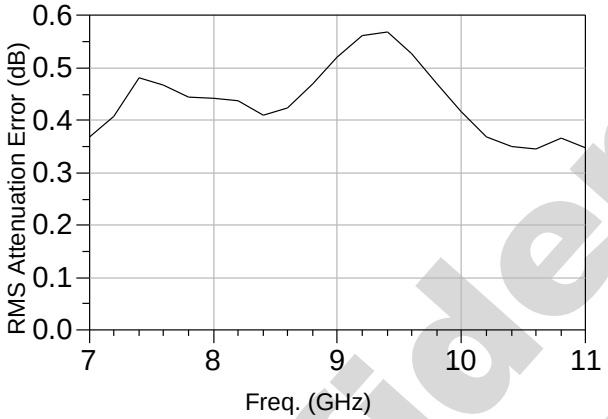




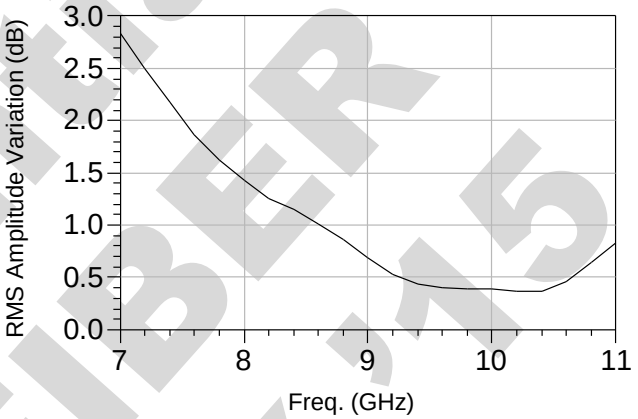


Attenuation Errors

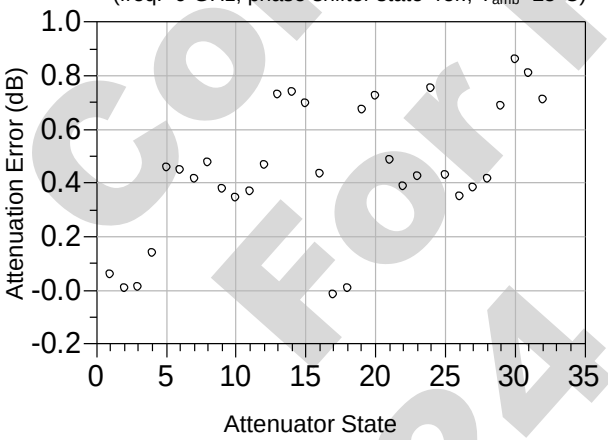
RMS Attenuation Error wrt Attenuator State
(for all 32 attenuation states, phase shifter state=ref., T_{amb}=25°C)



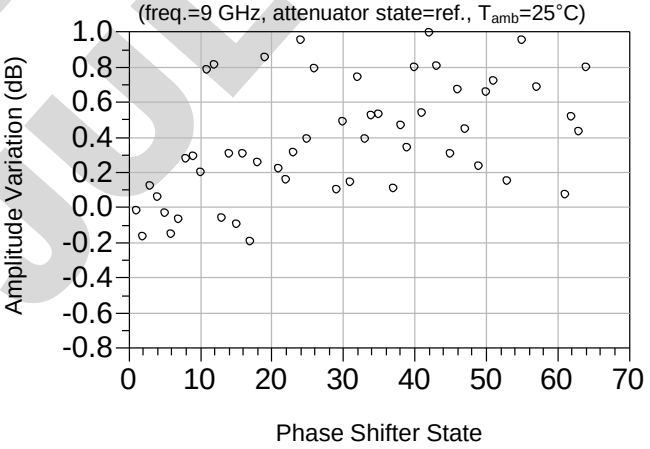
RMS Amplitude Variation wrt Phase Shifter State
(for all 64 phase shift states, attenuator state=ref., T_{amb}=25°C)



Attenuation Error wrt Attenuator State
(freq.=9 GHz, phase shifter state=ref., T_{amb}=25°C)

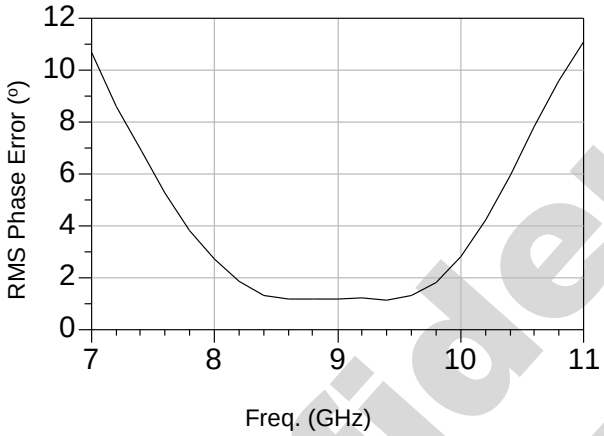


Amplitude Variation wrt Phase Shifter State
(freq.=9 GHz, attenuator state=ref., T_{amb}=25°C)

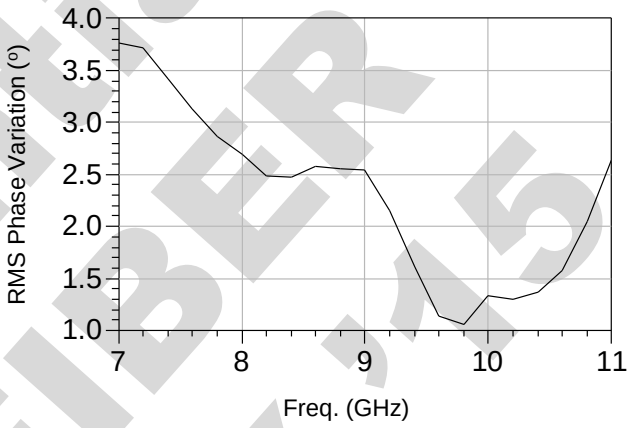


Phase Shifting Errors

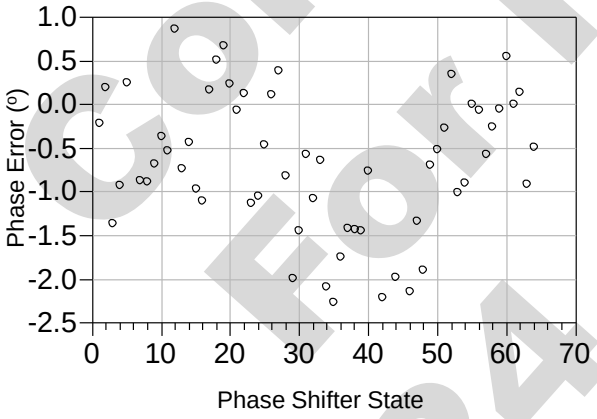
RMS Phase Error wrt Phase Shifter State
(for all 64 phase shift states, attenuator state=ref., T_{amb}=25°C)



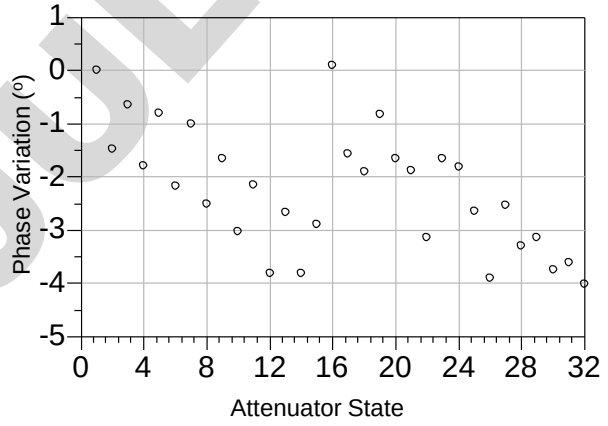
RMS Phase Variation wrt Attenuator State
(for all 32 attenuation states, phase shifter state=ref., T_{amb}=25°C)



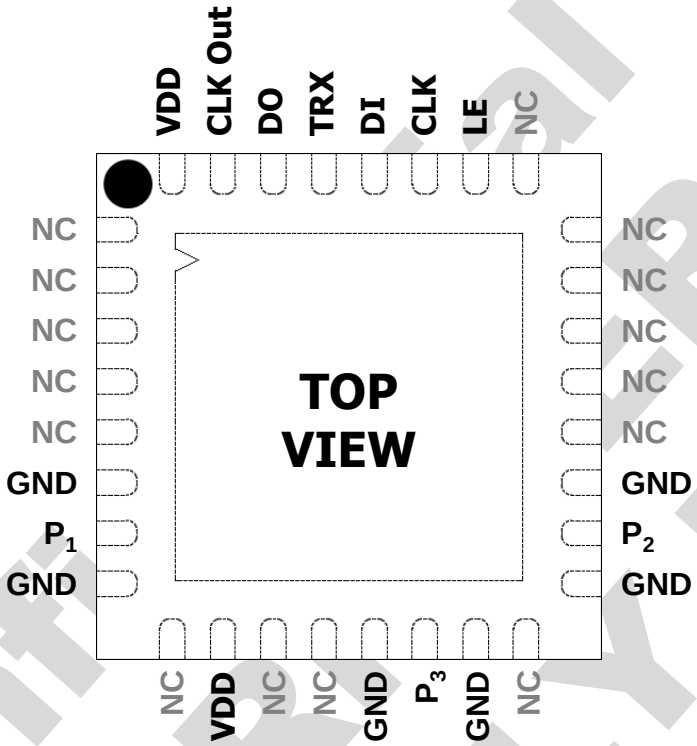
Phase Error wrt Phase Shifter State
(freq.=9 GHz, attenuator state=ref., T_{amb}=25°C)



Phase Variation wrt Attenuator State
(freq.=9 GHz, phase shifter state=ref., T_{amb}=25°C)



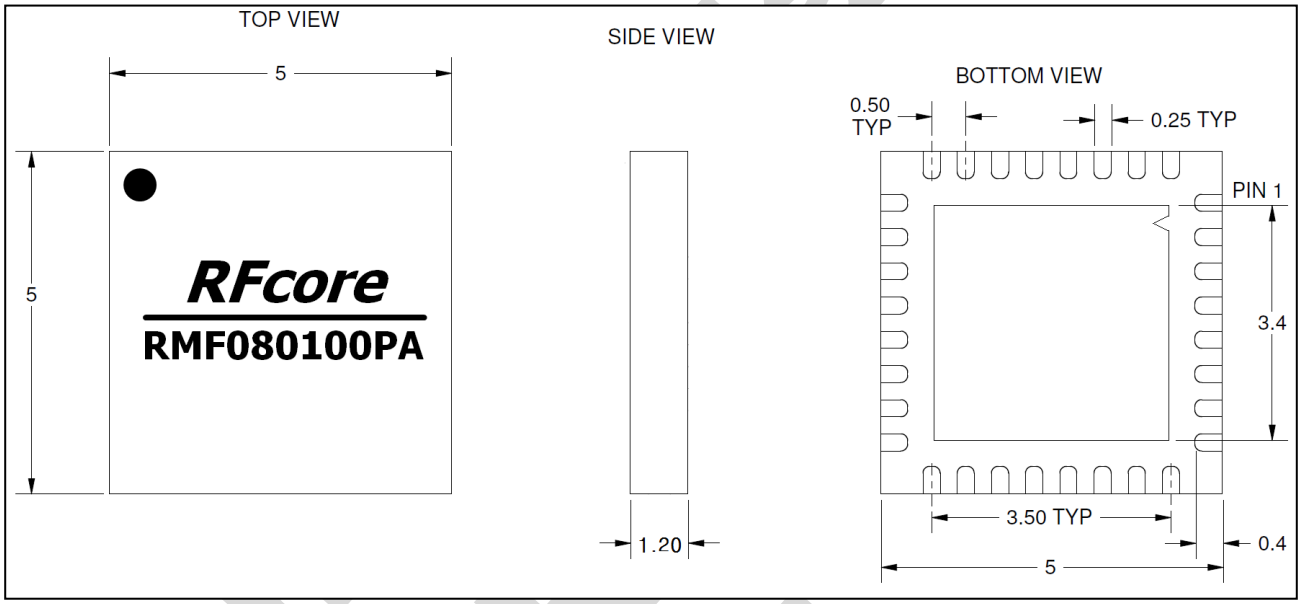
Pin Configuration



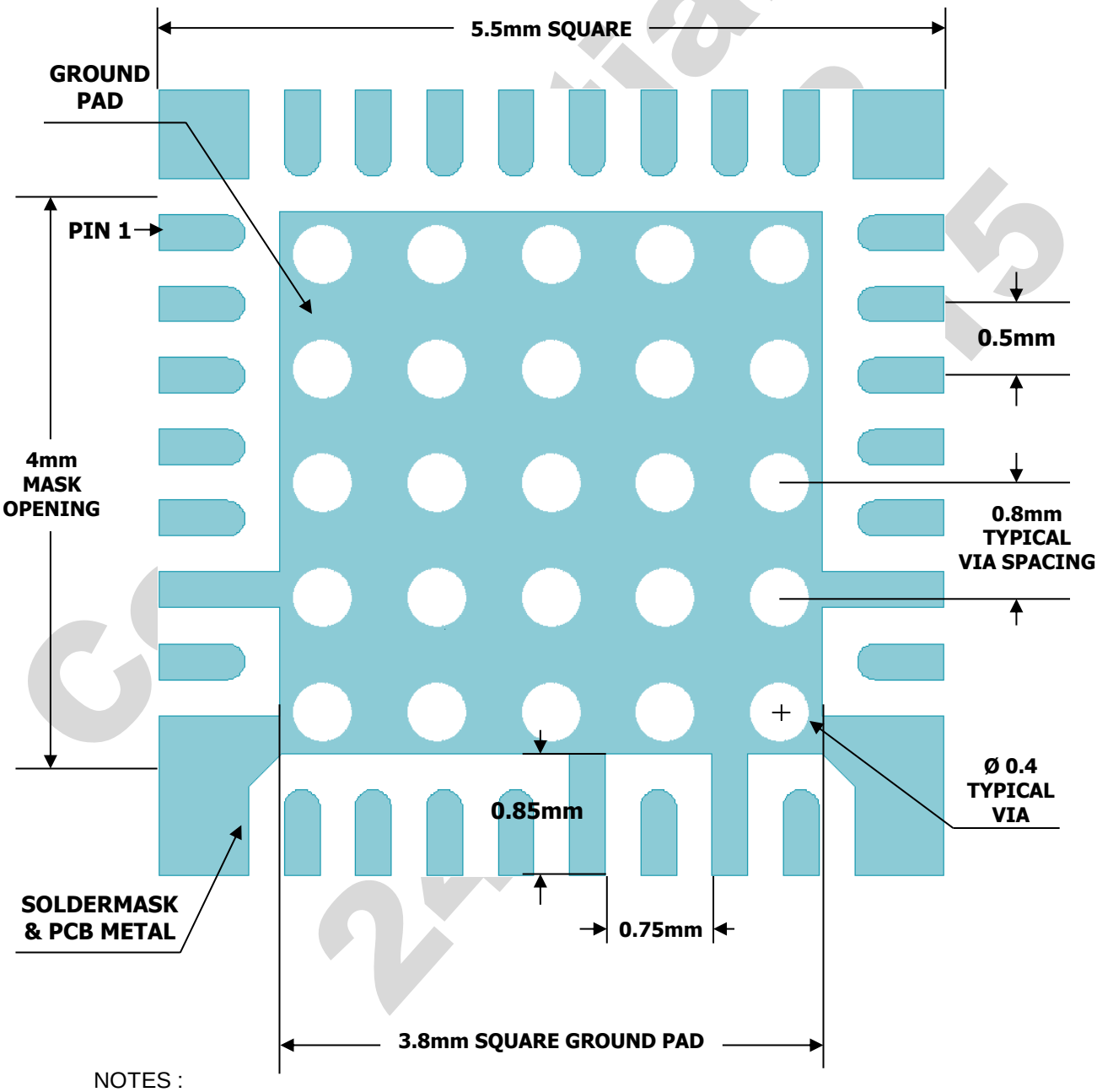
Symbol	Description	Recomended Operating Conditions
P_1	Tx in / Rx out	Z_0 = 50Ω
P_2	Tx out	Z_0 = 50Ω
P_3	Rx in	Z_0 = 50Ω
VDD	Power Supply	3.3V I_{DC}=250mA (TX), I_{DC}=100mA (RX)
DI	SPI Data In	Low=0V, High=3.3V
DO	SPI Data Out	Low=0V, High=3.3V
CLK	CLK for SPI	Low=0V, High=3.3V
LE	SPI Latch Enable	Low=0V, High=3.3V
TRX	Transmit / Receive mode control	Low=0V, High=3.3V
CLK Out	CLK Out	Low=0V, High=3.3V
N/C	Not Connected	Not Connected
GND	Ground	Ground

Package Outline

Type	Description	Terminals	Pitch (mm)	Package Size (mm}
QFN	Quad Flat No lead with exposed heat sink	32	0.5	5 x 5 x 1.2



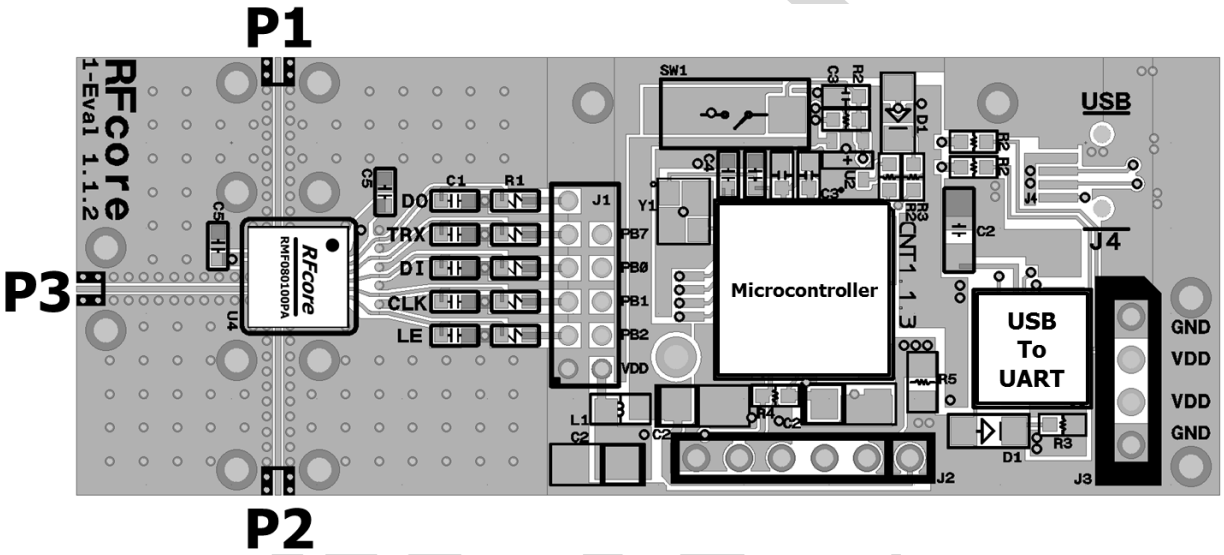
Suggested PCB Land Pattern



NOTES :

1. DIMENSIONS ARE IN MILLIMETERS.
2. PAD WIDTH SHOWN IS FOR SOLDERING ONLY. BEYOND SOLDERING AREA ALL CONDUCTORS THAT CARRY RF AND MICROWAVE SIGNALS SHOULD HAVE 50 OHM CHARACTERISTIC IMPEDANCE.

Evaluation Module (RMF080100PA-EVM)

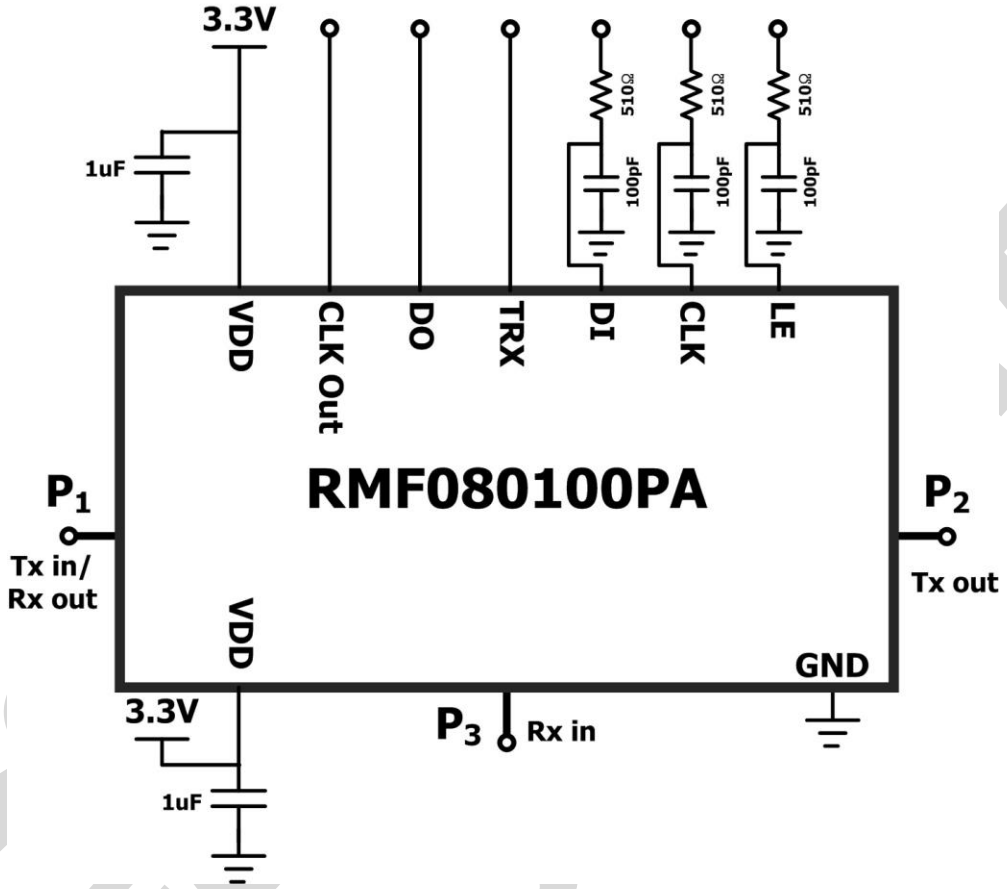


-The evaluation module is an easy to use platform for evaluating the X-band core chip RMF080100PA. The user can evaluate the performance of the RMF080100PA using a PC with USB interface and GUI software. The RMF080100PA-EVM includes the evaluation software on a CD-ROM.

Ordering Information

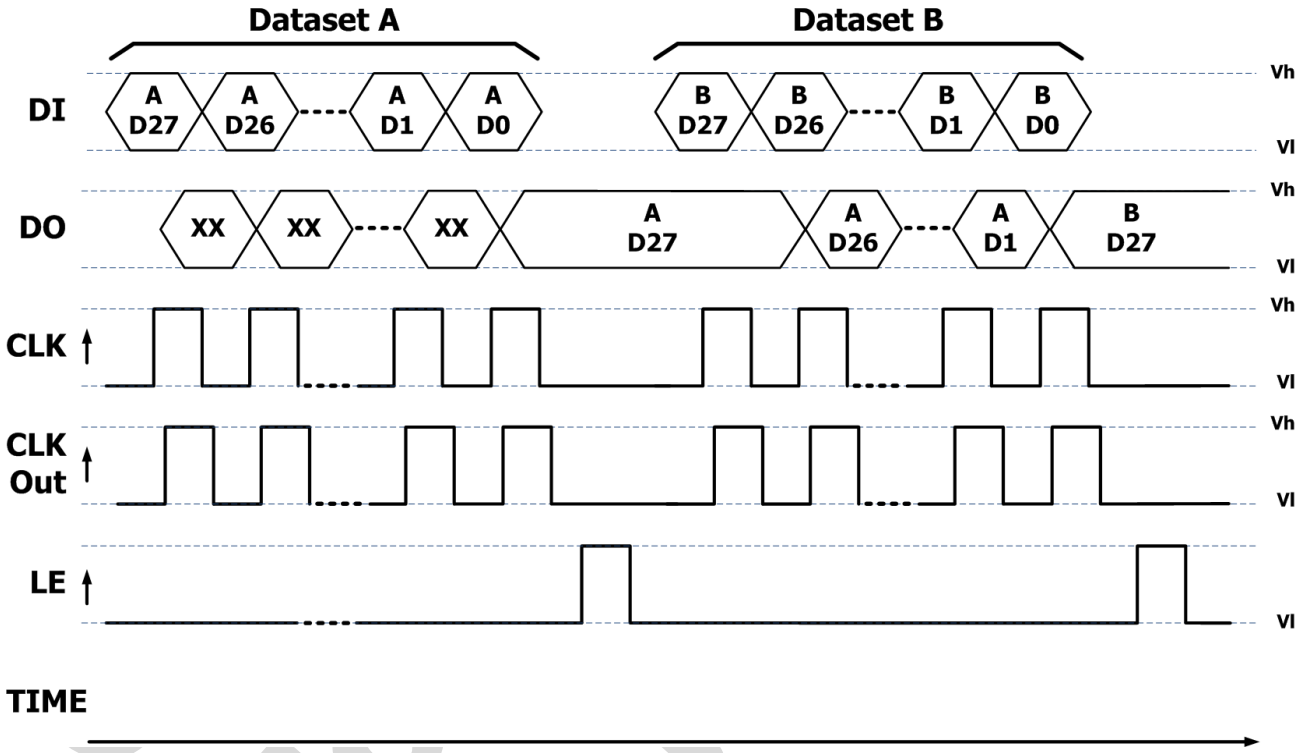
Item	Contents	Part Number
Evaluation Kit	RMF080100PA Core Chip Evaluation PCB mini USB Interface Board USB A Male to Mini USB 5Pin B Male 1.8M CD ROM (Evaluation Module User Guide, Evaluation Software)	RMF080100PA-EVM

Application Circuit



Time Diagram

- All functions are controlled by 28 bits of internal registers through serial interface.
- DI is sampled at the rising edge of CLK.
- LE must occur when all the bits are loaded.
- DO is delayed by 28th CLK of DI.
- Logic Low (Vl) = 0 ~ 1.3 V
- Logic High (Vh)= 2.0 ~ 3.3 V



Control Data

Bit Number	Description	Reference State / Condition
D0	Tuning bit(attenuation)	High
D1	Tuning bit(attenuation)	High
D2	Attenuation	Low
D3	Attenuation	Low
D4	Attenuation	Low
D5	Attenuation	Low
D6	Attenuation	Low
D7	Attenuation	Low
D8	Tuning bit(phase)	Low
D9	Tuning bit(phase)	Low
D10	Phase	Low
D11	Tuning bit(phase)	Low
D12	Tuning bit(phase)	High
D13	Phase	Low
D14	Phase	Low
D15	Phase	Low
D16	Phase	Low
D17	Phase	Low
D18	Enable LDO	Low
D19	LDO Control	Low
D20	LDO Control	Low
D21	LDO Control	High
D22	Bias Control	Low
D23	Bias Control	Low
D24	Bias Control	High
D25	Transmit/Receive Mode Selection	Low=Internal Mode, (TRX mode is controlled by D26) High=External Mode, (TRX mode is controlled by TRX pin)
D26	Transmit/Receive Mode Control	Low=TX High=RX
D27	Enable MFC	Low=Disable High=Enable

Attenuator control table

Atten. State	Bit Num. / Atten.(dB)	D2	D3	D4	D5	D6	D7	D12
0	0	0	0	0	0	0	0	1
1	1	1	0	0	0	0	0	1
2	2	0	1	0	0	0	0	1
3	3	1	1	0	0	0	0	1
4	4	0	0	1	0	0	0	1
5	5	1	0	1	0	0	0	1
6	6	0	1	1	0	0	0	1
7	7	1	1	1	0	0	0	1
8	8	0	0	0	0	0	1	1
9	9	1	0	0	0	0	1	1
10	10	0	1	0	0	0	1	1
11	11	1	1	0	0	0	1	1
12	12	0	0	1	0	0	1	1
13	13	1	0	1	0	0	1	1
14	14	0	1	1	0	0	1	1
15	15	1	1	1	0	0	1	0
16	16	0	0	0	1	1	0	0
17	17	1	0	0	1	1	0	0
18	18	0	1	0	0	1	1	0
19	19	1	1	0	0	1	1	0
20	20	0	0	1	1	1	0	0
21	21	1	0	1	1	1	0	0
22	22	0	1	1	1	1	0	0
23	23	1	1	1	0	1	1	0
24	24	0	0	0	1	1	1	0
25	25	1	0	0	1	1	1	0
26	26	0	1	0	1	1	1	0
27	27	1	1	0	1	1	1	0
28	28	0	0	1	1	1	1	0
29	29	1	0	1	1	1	1	0
30	30	0	1	1	1	1	1	0
31	31	1	1	1	1	1	1	0

Phase shifter control table

Phase State	Bit Num. / Phase(°)	D0	D1	D8	D9	D10	D11	D13	D14	D15	D16	D17
0	0	1	1	0	0	0	0	0	0	0	0	0
1	5.625	0	1	0	0	1	0	0	0	0	0	0
2	11.25	1	0	1	1	0	0	1	0	0	0	0
3	16.875	0	0	1	1	1	0	1	0	0	0	0
4	22.5	1	1	1	0	0	0	0	1	0	0	0
5	28.125	0	1	1	0	1	0	0	1	0	0	0
6	33.75	1	0	1	1	0	0	1	1	0	0	0
7	39.375	0	1	1	1	1	0	1	1	0	0	0
8	45	1	1	0	1	0	0	0	0	1	0	0
9	50.625	0	1	1	0	1	0	0	0	1	0	0
10	56.25	0	1	1	1	0	1	0	0	1	0	0
11	61.875	0	0	1	1	1	1	0	0	1	0	0
12	67.5	1	1	0	1	0	0	0	1	1	0	0
13	73.125	1	1	0	1	1	0	0	1	1	0	0
14	78.75	1	0	1	1	0	0	1	1	1	0	0
15	84.375	0	1	1	1	1	0	1	1	1	0	0
16	90	0	1	0	1	0	0	0	0	0	1	0
17	95.625	0	1	1	0	1	0	0	0	0	1	0
18	101.25	0	1	1	1	0	1	0	0	0	1	0
19	106.875	0	1	1	0	0	1	1	0	0	1	0
20	112.5	1	1	1	1	0	0	0	1	0	1	0
21	118.125	0	1	1	1	1	0	0	1	0	1	0
22	123.75	1	0	0	1	1	0	1	1	0	1	0
23	129.375	1	0	1	1	0	1	1	1	0	1	0
24	135	0	1	1	1	0	0	0	0	1	1	0
25	140.625	0	1	1	1	1	0	0	0	1	1	0
26	146.25	0	0	1	0	1	1	0	0	1	1	0
27	151.875	0	0	0	1	1	1	1	0	1	1	0
28	157.5	1	0	1	1	0	0	0	1	1	1	0
29	163.125	1	0	1	1	1	0	0	1	1	1	0
30	168.75	0	1	1	1	0	0	1	1	1	1	0
31	174.375	0	1	1	0	0	1	1	1	1	1	0
32	180	1	1	0	0	0	0	0	0	0	0	1
33	185.625	1	0	0	1	1	0	0	0	0	0	1
34	191.25	0	1	1	1	0	0	1	0	0	0	1
35	196.875	0	1	1	1	1	0	1	0	0	0	1
36	202.5	1	0	1	1	0	0	0	1	0	0	1
37	208.125	0	1	1	1	1	0	0	1	0	0	1
38	213.75	0	1	1	1	0	0	1	1	0	0	1
39	219.375	0	1	1	1	1	0	1	1	0	0	1
40	225	1	0	1	1	0	0	0	0	1	0	1
41	230.625	1	0	1	1	1	0	0	0	1	0	1
42	236.25	0	0	0	0	0	1	1	0	1	0	1
43	241.875	0	0	0	0	1	1	1	0	1	0	1
44	247.5	1	0	1	1	0	0	0	1	1	0	1
45	253.125	1	0	1	1	1	0	0	1	1	0	1
46	258.75	0	1	1	1	0	0	1	1	1	0	1
47	264.375	0	1	0	1	0	1	1	1	1	0	1
48	270	1	0	1	0	0	0	0	0	0	1	1
49	275.625	1	0	1	0	1	0	0	0	0	1	1
50	281.25	0	1	1	1	0	0	1	0	0	1	1
51	286.875	0	1	1	1	1	0	1	0	0	1	1
52	292.5	1	0	1	1	0	0	0	1	0	1	1
53	298.125	1	1	1	1	1	0	0	1	0	1	1
54	303.75	1	1	1	1	0	0	1	1	0	1	1
55	309.375	1	0	0	1	0	1	1	1	0	1	1
56	315	1	0	1	1	0	0	0	0	1	1	1
57	320.625	1	0	1	1	1	0	0	0	1	1	1
58	326.25	1	0	0	0	0	1	1	0	1	1	1
59	331.875	0	0	0	0	1	1	1	0	1	1	1
60	337.5	1	0	0	1	0	0	0	1	1	1	1
61	343.125	1	0	0	1	1	0	0	1	1	1	1
62	348.75	1	0	1	1	0	0	1	1	1	1	1
63	354.375	1	0	1	1	1	0	1	1	1	1	1